TECHNICAL MANUAL

GENERAL SYSTEM

TACTICAL ELECTRONIC WARFARE SYSTEM

FMS SERIES
F-15C AND F-15D

WR-ALC/LFIT

This publication supersedes TO SR1F-15C-2-99GS-00-1 thru Change 8 dated 01 February 1998.

This publication is incomplete without classified TO SR1F-15C-2-99GS-00-2.

LIST OF EFFECTIVE PAGES

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11-16	0	11-62	0	13-28	0	13-74	0
11-17	0	11-63	0	13-29	0	13-75	0
11-18	0	11-64	0	13-30	0	13-76	0
11-19	0	11-65	0	13-31	0	13-77	0
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INTRODUCTION

PURPOSE AND SCOPE.

This technical manual is one of a series providing maintenance instructions for the F-15C and F-15D aircraft. Maintenance instructions are compatible with the provisioning of spare parts, test equipment and special tools. This manual provides descriptions and principles of operation for the tactical electronics warfare system (TEWS), which is made up of the subsystems below:

Radar Warning Receiver (RWR) - AN/ALR-56C

Internal Countermeasures System (ICMS) -

AN/ALQ-135E(V)

Interference Blanker

Countermeasures Dispenser Set (CMD) - AN/ALE-45

Test equipment, consumable supplies and special tools required for servicing and maintenance are listed.

Five digit codes used throughout this publication to identify equipment manufacturer may be designated as Mfg. Code, FSCM or CAGE.

SIGNIFICANT CHANGES.

The significant changes in this revision are the removal of the PREMSIP data and drawings and incorporation of F-15C/D Suite 2 data.

APPLICABILITY NOTATIONS.

Information and instructions contained in this manual unique to one model are identified as F-15C or F-15D. Data applicable to specific aircraft within a series are identified by RSAF serial number.

IMPROVEMENT REPORTS.

Recommendations for improvements to this technical order shall be submitted on AFTO Form 22, Technical Order System Publication Improvement Report, in accordance with TO 00-5-19. Completed forms shall be forwarded to WR-ALC/LFI, 296 COCHRAN STREET, ROBINS AFB, GA 31098-1622.

RECORD OF APPLICABLE TIME COMPLIANCE TECHNICAL ORDERS.

The record of applicable time compliance technical orders is a list of all TCTO's which affect the technical content (text or illustration) of this manual. Only current TCTO's are listed. A TCTO is deleted from the list when any of the below occurs:

a. The equipment configuration to which the TCTO is applicable is no longer covered in the manual.

b. The TCTO is rescinded.

c. The TCTO is superseded or replaced.

Record of Applicable Time Compliance Technical Orders

TCTO No.	Title	TCTO Date
SR1F-15-1019	Increased High Pressure Water Separator (ECP MDA-F-15-1617R1-OW)	30 November 1992

SECTION 00

TACTICAL ELECTRONIC WARFARE SYSTEM (TEWS)

00-1. **SYSTEM FUNCTIONAL DESCRIPTION.**

00-2. **DESCRIPTION.** Refer to figure 00-1.

00-3. This section describes the overall aspects of the F-15 aircraft Tactical Electronic Warfare System (TEWS).

00-4. The primary function of the TEWS system is to provide defensive and offensive electronic warfare ability for the F-15 aircraft under various tactical environments. The TEWS system is several related subsystems integrated into one system, with automatic or pilot-initiated reaction to any threat situation.

00-5. **Radar Warning Receiver (RWR).** The RWR subsystem receives, analyzes and stores threat data transmitted by surface-to-air missiles (SAM), air intercept (AI), anti-aircraft artillery (AAA) control and communication systems. The stored data is provided to the pilot as warning lamp and CRT displays to enable determination of the threat situation.

00-6. The RWR also provides automatic control and tuning data for the Internal Countermeasures Set (ICMS) and Countermeasures Dispenser Set (CMD).

00-7. **Internal Countermeasures Set (ICMS) (F-15C).** The ICMS contains three separate sets (band 1, 2 and 3) that provide jamming ability against threat signals. Band 1 and 2 jamming parameters are derived either by automatic program control under the direction of the RWR, or by fixed, repeating parameter control by a self-contained program. Band 3 operates in two modes auto (normal) and manual (emergency). During band 3 set operation in the auto mode, the RWR provides threat information for comparison with threat information obtained by the band 3 set. During manual operation, the RWR RF environment threat information is used.

00-8. **Interference Blanker (Blanker).** The blanker is a maintenance-programmable device that suppresses the responses of the RWR and other on-board receiving equipment to electronic interference from on-board transmitting equipment.

00-9. **Tactical Electronic Warfare Pod (TEWS Pod).** The TEWS pod is used as an auxiliary to the TEWS system to extend the abilities of the internal TEWS system. The TEWS pod is carried externally on station 5 (centerline).

00-10. **Countermeasures Dispenser Set AN/ALE-45 (CMD).** The CMD counters most immediate threats by dispensing chaff, IR flare, and/or other expendable countermeasure payloads.

00-11. **Transmission Line Testing.** Refer to TO SR1F-15C-2-99GS-00-2.

00-12. **SPECIAL MAINTENANCE REQUIREMENTS.** Refer to TO SR1F-15C-2-99GS-00-2.

00-13. **RF TRANSMISSION LINE/WAVEGUIDE/ RF COMPONENT TEST PROCEDURES.** Refer to TO SR1F-15C-2-99GS-00-2.

00-14. **CONSUMABLE MATERIALS LIST.** Refer to TO SR1F-15C-2-99GS-00-2.

00-15. **SUPPORT EQUIPMENT LIST.** Refer to TO SR1F-15C-2-99GS-00-2.

00-16. **TEST EQUIPMENT.** Refer to TO SR1F-15C -2-99GS-00-2.

LEGEND

[1] F-15C.

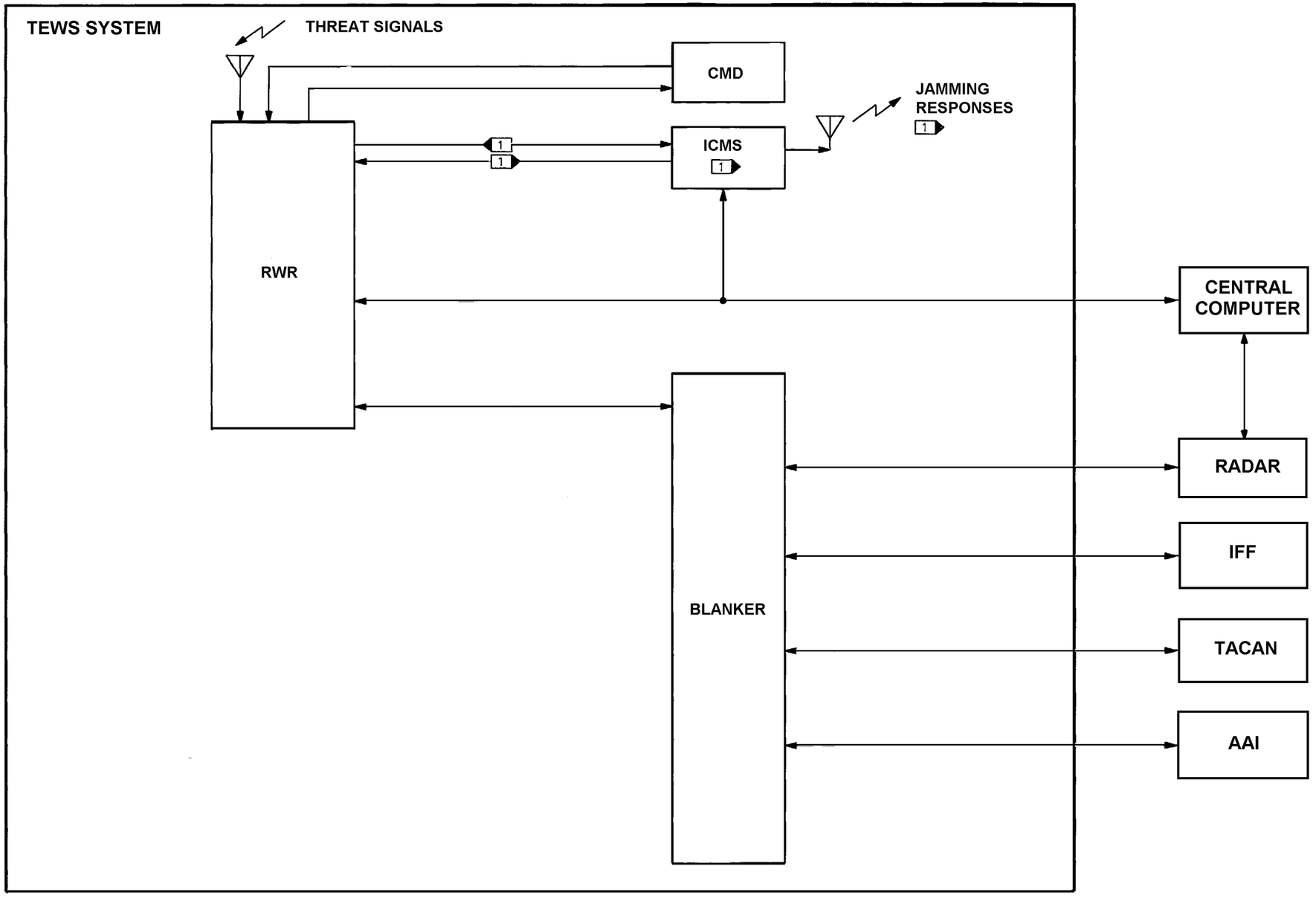


Figure 00-1. TEWS Block Diagram.

SECTION XI

RADAR WARNING RECEIVER SET AN/ALR-56C (RWR)

11-1. SYSTEM FUNCTIONAL DESCRIPTION.

11-2. This section contains maintenance instructions for Radar Warning Receiver Set AN/ALR-56C (RWR), which includes equipment listed in Table 11-1 installed on the F-15C and F-15D aircraft. The RWR is one of the subsystems which makes up the tactical electronic warfare system (TEWS).

11-3. The primary function of the RWR is to detect RF from enemy fire control radar systems (threats). After detection, the RWR uses this information to process and classify threats and provide jammer management. An audible tone and visual display are produced by the RWR to attract attention to the detected threats and threat location. Determination of jamming requirements is made by comparison of received signals and a stored program threat table. The RWR has a multiple function built-in test (BIT).

11-4. **DESCRIPTION.** See Figures 11-1 and 11-2. The RWR, under programmed control, detects and analyzes RF threats. After detection, the information is used to control jamming against RF transmitting devices that show a threat to the aircraft. RF energy is received through one or more combinations of five antennas and provided to the high band or low band receiver.

11-5. Signal Processing. The digitally controlled, low and high band, superheterodyne receivers convert the RF to the required IF. The IF is routed to the processor section of the low band receiver/processor where the received RF intelligence (frequency spectrum) is detected, processed and digitized for transfer to the computer in the power supply. The computer analyzes the digitized information for possible threat transmissions. A match between the received RF sample and a frequency in the threat spectrum will call for threat evaluation.

11-6. A computer program enables circuitry in the low band receiver/processor to digitize suspect RF for analysis by the computer to identify potential threats. A threat signal causes the RWR to produce visual and audio warning signals and to automatically activate applicable jamming transmitters in the internal countermeasures set (ICMS).

11-7. The RWR BIT verifies hardware and software integrity through C-BIT (continuous BIT), P-BIT (periodic BIT), I-BIT (initiated BIT). It also has a MAINT BIT function that displays a record of RWR BIT failures and a pilot BIT that allows the pilot to monitor the system in-flight.

a. C-BIT monitors system computer memory parity, the system deadman timer (DMT), and the receiver scan. In the event of power fluctuations, memory parity errors, DMT activation, or scan hang-up, BIT interrupts system processing to perform fault isolation.

b. P-BIT, also called automatic BIT, invoked by the OFP verifies the operation of the AN/ALR-56C system by doing periodic tests of RWR functions. The complete BIT set has three segments, with one segment performed approximately every four seconds (all three segments are completed approximately every twelve seconds). Some functions, however, require more than one cycle for a complete test. A full system test is completed approximately every minute. Its general approach is to verify that an end to end RWR function is working (excluding actual antenna reception capability), rather than checking individual LRU's or hardware components.

c. I-BIT, also called manual BIT, initiates a check on the system computer and its memory and verifies the integrity of the software load. It also provides a graphic display of symbology on the TEWS Display for approximately five seconds, then a second display appears for approximately four seconds indicating the word RANCH, brackets and three lines of numbers that represent the RWR OFP, Band 2 ICMS OFP and Band 3 ICMS OFP. In addition, the launch and caution tones can be heard through the headsets.

d. Maintenance BIT displays matrix "B" (confirmed failures). These failures have been confirmed by the double 5/7 rule and will be displayed with flight write prom data (failures detected in flight). Access to this feature of BIT is provided by initiating manual BIT and cycling the RWR/ICS switch on the TEWS IA control panel between the COMBAT and TRAINING modes.

11-8. **LINE REPLACEABLE UNITS.** RWR system line replaceable units (LRU) are identified and listed in Table 11-1.

11-9. **COMPONENT DESCRIPTION.** The paragraphs below describe the RWR units. Each unit is hard-mounted and, where required, cooled by the aircraft environmental control system (ECS) that provides air flow to dissipate heat.

11-10. **High Band Receiver (99-11-10).** The high band receiver detects high band RF transmissions and processes them to be analyzed in the low band receiver/ processor. The high band transmissions are also used in the direction finding function of the RWR.

11-11. **Low Band Receiver/Processor (99-11-11).** The low band receiver/processor detects and processes low band transmissions. These transmissions along with high band transmissions are processed and digitized for transfer to the computer in the power supply.

11-12. **Power Supply (99-11-12).** The power supply converts 115vac, 400 Hz, 3Ø aircraft power to the required ±DC voltages used by the RWR system. The +28vdc aircraft voltage is used for control. An internal computer analyzes digitized low band and high band transmissions to determine all threat parameters.

11-13. **TEWS Display Unit (99-11-13).** The TEWS display unit visually displays the threat environment.

11-14. **TEWS Control Panel (99-11-14).** The TEWS control panel controls the operation of the TEWS.

11-15. **TEWS IA Control Panel (99-11-15).** The TEWS IA control panel controls the operational modes of the TEWS.

11-16. **Low Band Antenna (99-11-16).** The low band antenna has a single omnidirectional element with a resistively coupled tap for BIT use.

11-17. **Left Fin Antenna (99-11-17).** The left fin antenna is used for RF detection and direction finding with the other three high band antennas.

11-18. **Left Wing Antenna (99-11-18).** The left wing antenna is used for RF detection and direction finding with the other three high band antennas.

11-19. **Right Fin Antenna (99-11-19).** The right fin antenna is used for RF detection and direction finding with the other three high band antennas.

11-20. **Right Wing Antenna (99-11-20).** The right wing antenna contains two elements. One element is used for RF detection and as an elevation reference for the direction finding function of the system. The other element is used for RF detection and direction finding with the other three high band antennas. The four high band antennas form an omnidirectional pattern around the aircraft each defining 90 degrees of azimuth.

11-21. **Cable Assembly(ies) (99-11-21 thru 99-11-32).** Six cable assemblies transfer RF signals detected by the RWR antennas to the receiving circuits in the high band receiver and low band receiver/ processor. The other cable assemblies provide system interface connections. Refer to Table 11-1.

11-22. **PRINCIPLES OF OPERATION.** See Figure 11-2. The RWR principles of operation are shown as a description of operating controls and indicators, and operation of the system functions as below:

a. Power Distribution

b. Receiving Circuits

c. Computer/Processor

d. Threat Processing Circuits

e. Display Circuits

f. Warning Lights and Audio Circuits

g. BIT Circuits

h. System Interface

11-23. **Controls and Indicators.** All controls and indicators used in RWR operation are shown in Figure 11-1 and described in Table 11-2.

1-24. **Display Symbols.** Classified secret. Refer to TO SR1F-15C-2-99GS-00-2, section 11.

11-25. **Cockpit Light Indicators.** Classified secret. Refer to TO SR1F-15C-2-99GS-00-2, section 11.

11-26. **Power Distribution.** See Figure 11-3. Primary power of 115vac, 400 Hz, 3 Ø and 28vdc is routed to the power supply, while 28vdc only is routed to the TEWS control panel. When external electrical power is applied to the aircraft and before the RWR system is turned on, the RWR light on the BCP is on. RWR power on is done by turning the RWR switch on the TEWS control panel to the ON position. The 28vdc supply is routed from the power supply through the deenergized contacts of avionics protection relay no. 5 (52K-J280) to the control panel. This relay energizes, removing power from RWR, if there is not enough

Table 11-1. Line Replaceable Units

Common Name	S/S/SN	Ref. Des.	Nomenclature
[1] AI Light Relay	39-40-22	55K-Y008	Relay
[1] SAM Light Relay	39-40-22	55K-Y006	Relay
High Band Receiver (LRU-6)	99-11-10	64RET005	Countermeasures Receiver, R-2245/ALR-56C
Low Band Receiver/Processor (LRU-3)	99-11-11	65RED002	Countermeasures Receiver, R-2244/ALR-56C
Power Supply (LRU-2)	99-11-12	65PSD001	Power Supply PP-7855/ALR-56C
TEWS, Display Unit (LRU-9)	99-11-13	65Z-J009	Countermeasures Display IP-1164B/ ALR-56
TEWS, Control Panel (LRU-10)	99-11-14	65Z-J010	Receiver Control C-9428/ALR-56
TEWS IA Control Panel (LRU-11)	99-11-15	65Z-H011	Receiver Control C-9429/ALR-56
Low Band Antenna (LRU-8)	99-11-16	65E-G008	Antenna AS-2934/ALR-56
Left Fin Antenna (LRU-7L)	99-11-17	65E-S007	Antenna Group OE-169/ALR-56
Left Wing Antenna (LRU-5L)	99-11-18	65E-U004	Antenna Group OE-167/ALR-56
Right Fin Antenna (LRU-7R)	99-11-19	65E-T006	Antenna Group OE-168/ALR-56
Right Wing Antenna (LRU-5R)	99-11-20	65E-V003	Antenna Group OE-166/ALR-56
BIT Cable Assembly (SW289A)	99-11-21	65E-G008	Cable Assembly (SW289A)
[2] RF Sample Cable Assembly	99-11-22	TE186A	Cable Assembly (TE186A)
[2] RF Sample Cable Assembly	99-11-23	TE186B	Cable Assembly (TE186B)
[2] RF Sample Cable Assembly	99-11-24	TE186C	Cable Assembly (TE186C)
Cable Assembly	99-11-25	65W-R501	Cable Assembly (SW1A)
Cable Assembly	99-11-26	65W-V502	Cable Assembly (SW2A)
Cable Assembly	99-11-29	65W-V503	Cable Assembly (SW3A)
Cable Assembly	99-11-30	65W-U504	Cable Assembly (SW4A)
Cable Assembly	99-11-31	65W-T506	Cable Assembly (SW5A)
Cable Assembly	99-11-32	65W-S507	Cable Assembly (SW6A)
BIT Cable Assembly (SW289B)	99-11-33	65E-G008	Cable Assembly (SW289B)

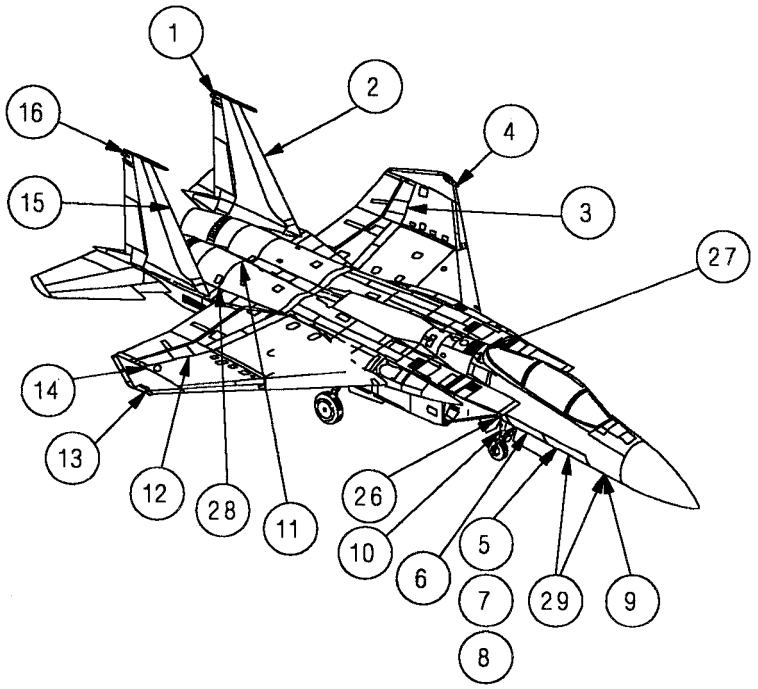
[1] F-15D
[2] F-15C

LEGEND

1 RELATED TO BUT NOT PART OF RADAR WARNING RECEIVER

2 F-15C

3 F-15D



INDEX NO.	COMMON NAME	S/S/SN	REF DES	ACCESS
1	LEFT FIN ANTENNA	99-11-17	65E-S007	LEFT VERTICAL STABILIZER
2	CABLE ASSEMBLY	99-11-32	65W-S507	AFT FUSELAGE AND LEFT FIN
3	CABLE ASSEMBLY	99-11-30	65W-U504	LEFT WING
4	LEFT WING ANTENNA	99-11-18	65E-U004	LEFT WING TIP
5	CABLE ASSEMBLY	99-11-25	65W-R501	NLG FORWARD DOOR AND DOOR 6R
6	RIGHT BUS CIRCUIT BREAKER PANEL NO. 1	24-50-17	52Z-F005	DOOR 10R
7	LOW BAND RECEIVER/PROCESSOR	99-11-11	65RED002	DOOR 6R
8	POWER SUPPLY	99-11-12	65PSD001	DOOR 6R
9	LOW BAND ANTENNA	99-11-16	65E-G008	NLG FORWARD DOOR
10	AVIONICS STATUS PANEL	31-50-18	66Z-G001	NOSE WHEELWELL
11	HIGH BAND RECEIVER	99-11-10	65RET005	DOOR 197
12	CABLE ASSEMBLY	99-11-29	65W-V503	RIGHT WING
13	RIGHT WING ANTENNA	99-11-20	65E-V003	RIGHT WING TIP
14	CABLE ASSEMBLY	99-11-26	65W-V502	RIGHT WING
15	CABLE ASSEMBLY	99-11-31	65W-T506	AFT FUSELAGE AND RIGHT FIN
16	RIGHT FIN ANTENNA	99-11-19	65E-T006	RIGHT VERTICAL STABILIZER
17	MAIN COMM CONTROL PANEL	23-24-30	90Z-J010	COCKPIT
18	TEWS DISPLAY UNIT	99-11-13	65Z-J009	COCKPIT
19	TEWS CONTROL PANEL	99-11-14	65Z-J010	COCKPIT
1 3 20	REAR INTEGRATED COMM CONTROL PANEL	23-24-29	78Z-K017	REAR COCKPIT
1 3 21	AVIONICS REPLAY PANEL 4	39-40-22	55Z-Y013	REAR COCKPIT
1 3 22	REAR MAIN COMM CONTROL PANEL	23-24-31	78Z-L030	REAR COCKPIT
1 23	BIT CONTROL PANEL	31-50-11	66Z-H002	COCKPIT
1 24	INTEGRATED COMM CONTROL PANEL	23-24-28	78Z-H001	COCKPIT
25	TEWS IA CONTROL PANEL	99-11-15	65Z-H011	COCKPIT
2 26	RF SAMPLE CABLE ASSEMBLY	99-11-22	TE-186A	AFT FUSELAGE AND ECS BAY
2 27	RF SAMPLE CABLE ASSEMBLY	99-11-23	TE-186B	NO. 5 EQUIPMENT COMPARTMENT
2 28	RF SAMPLE CABLE ASSEMBLY	99-11-24	TE-186C	AFT FUSELAGE
29	BIT CABLE ASSEMBLY	99-11-21	SW289A	NLG FOWARD DOOR AND DOOR 6R
1 30	MULTIPURPOSE COLOR DISPLAY	94-10-27		COCKPIT

TCG/15-03-00

Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 1 of 6)

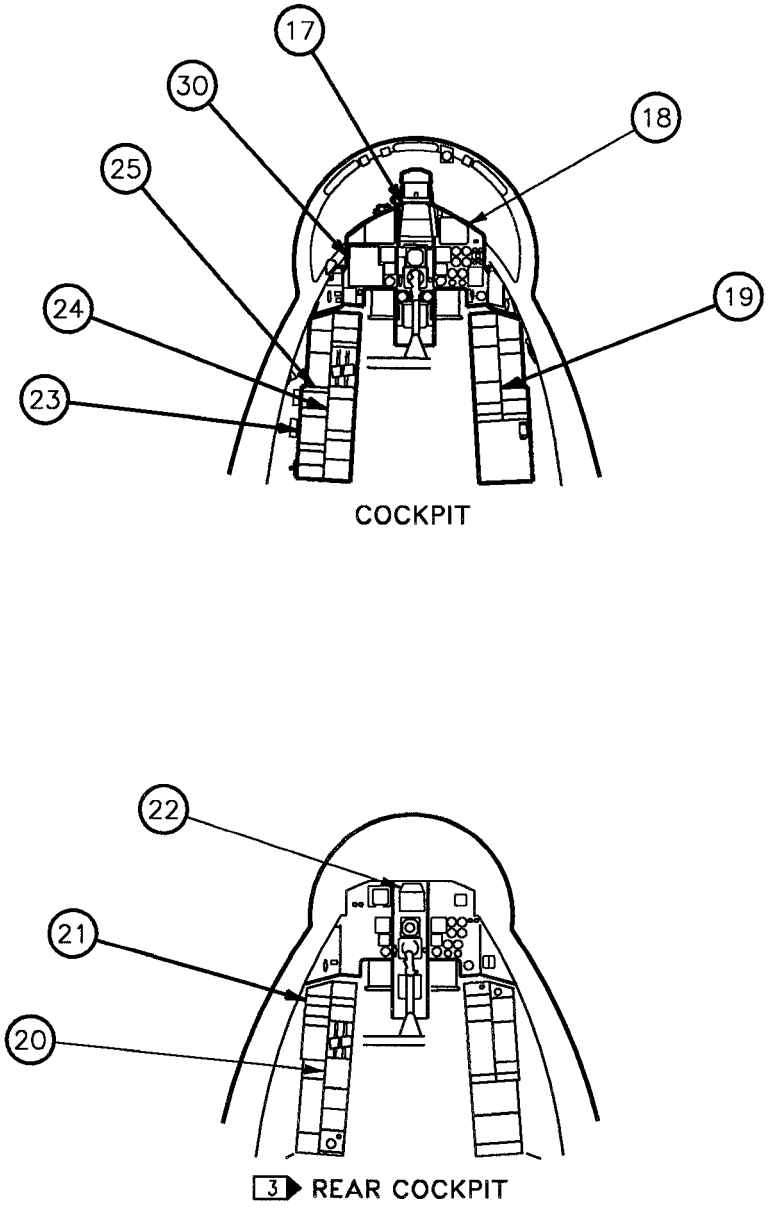
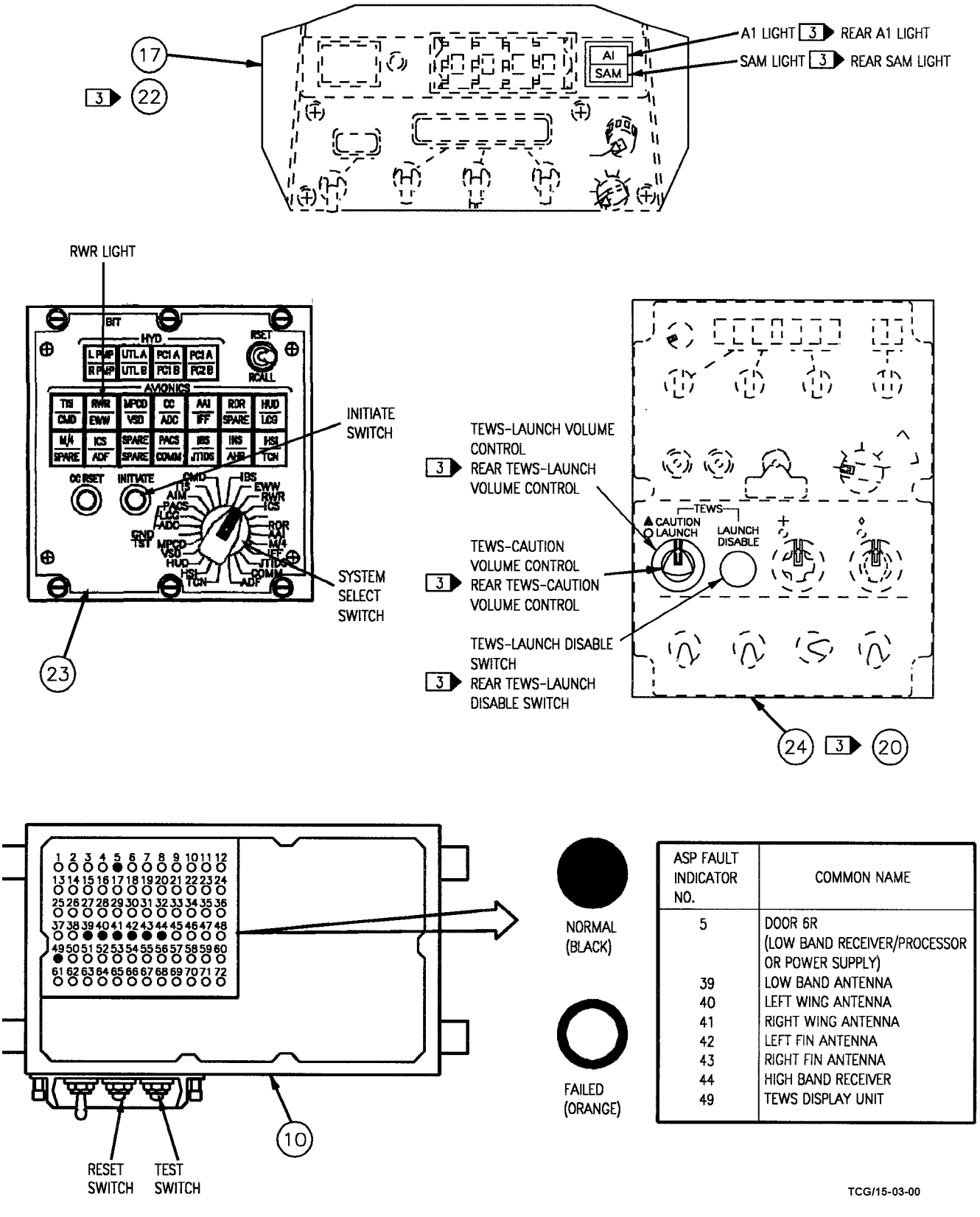


Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 2)



ASP FAULT INDICATOR NO.	COMMON NAME
5	DOOR 6R (LOW BAND RECEIVER/PROCESSOR OR POWER SUPPLY)
39	LOW BAND ANTENNA
40	LEFT WING ANTENNA
41	RIGHT WING ANTENNA
42	LEFT FIN ANTENNA
43	RIGHT FIN ANTENNA
44	HIGH BAND RECEIVER
49	TEWS DISPLAY UNIT

Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 3)

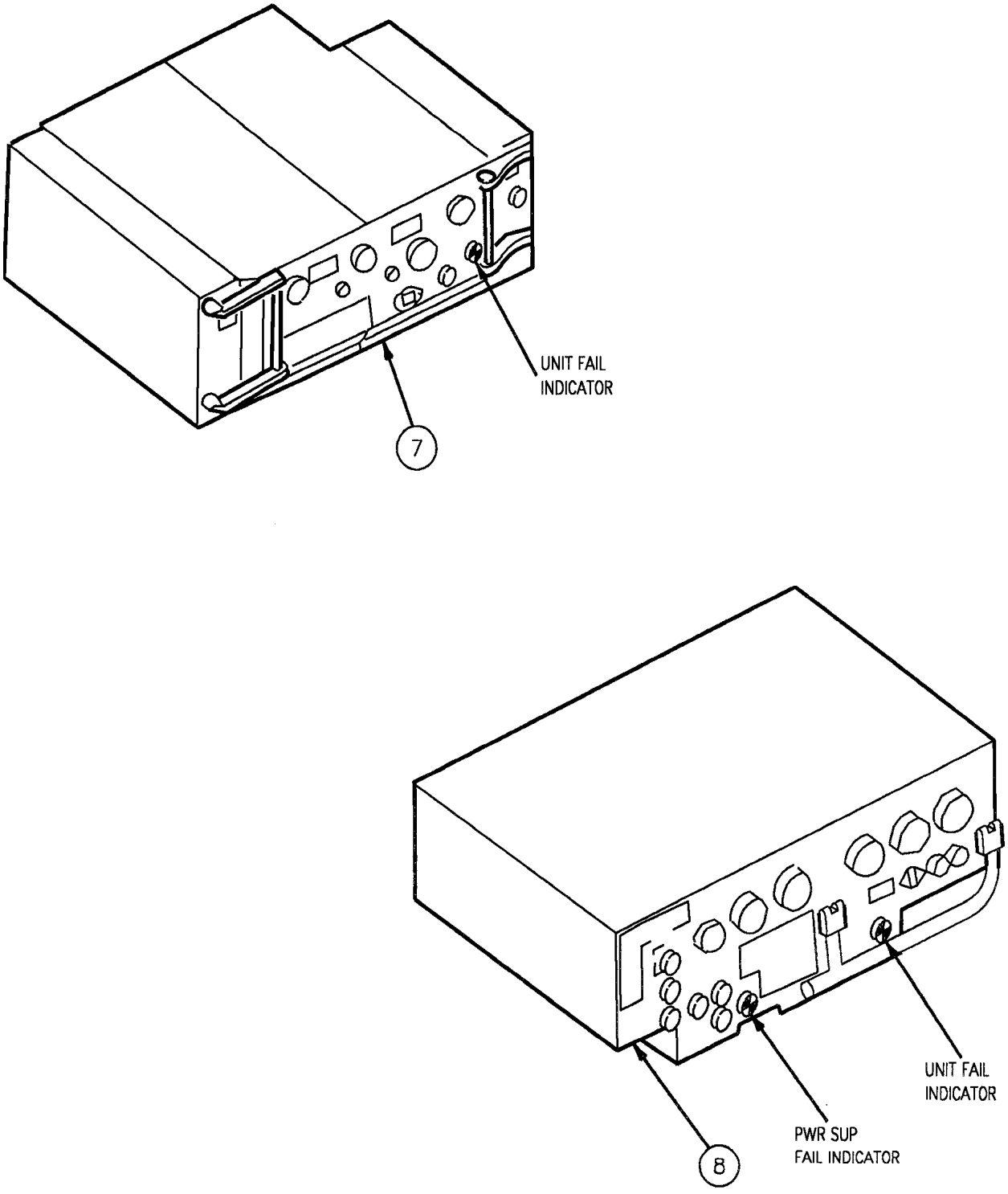


Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 4)

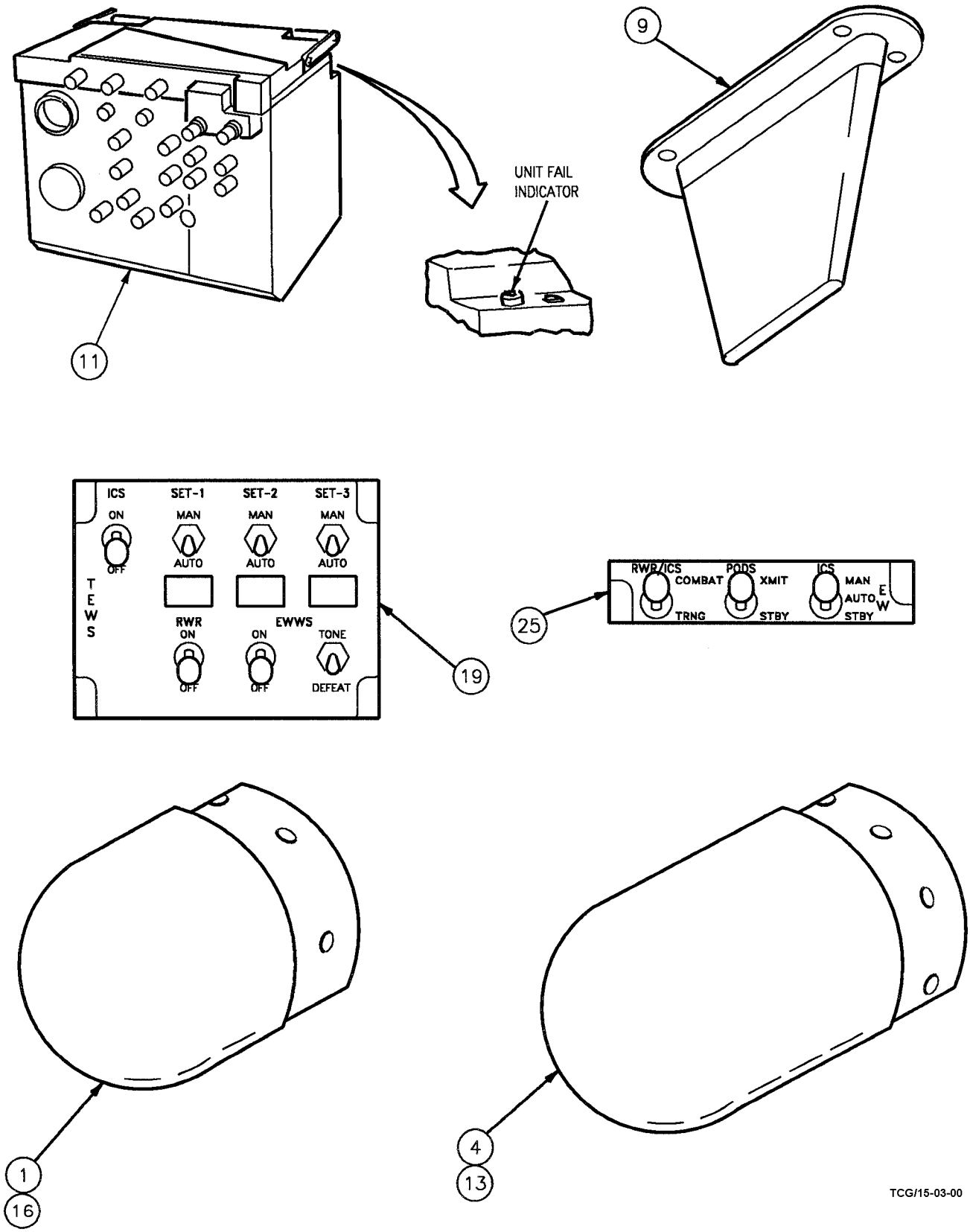
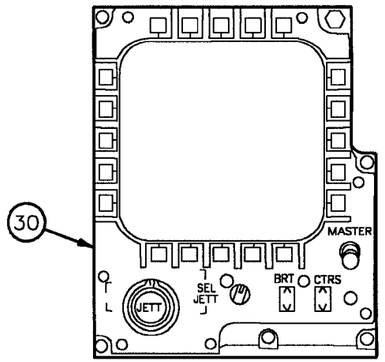
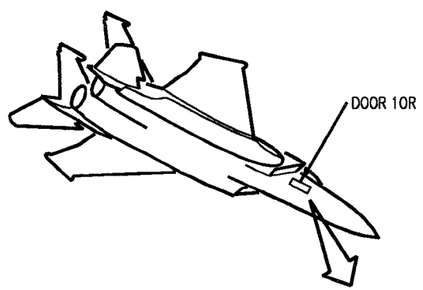
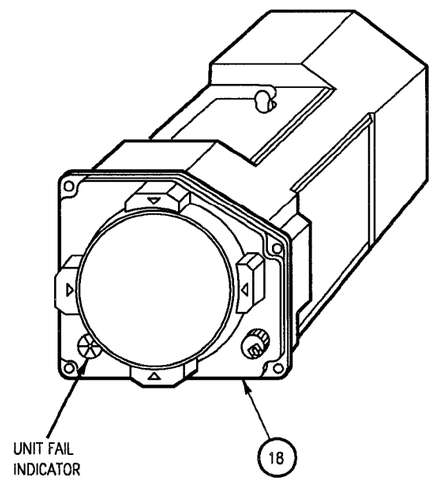


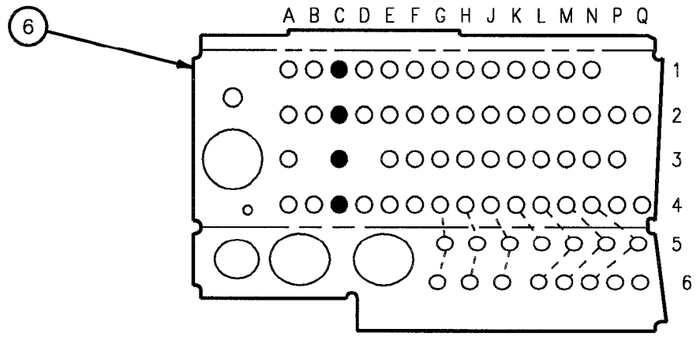
Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 5)



1 MULTIPURPOSE COLOR DISPLAY (MPCD)







52Z-F005

52Z-F005 RIGHT CIRCUIT BREAKER PANEL NO.1 (24-50-17)			
REF DES	ZONE	NOMENCLATURE	BUS
65CBF020	E1	115VØA RDR WRN RCVR PWR	R 115VACØA
65CBF021	E2	115VØB RDR WRN RCVR PWR	R 115VACØB
65CBF022	E3	115VØC RDR WRN RCVR PWR	R 115VACØC
65CBF024	E4	28VDC RDR WRN RCVR PWR	R 28VDC

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Figure 11-1. Countermeasures Receiving Set AN/ALR-56C (Sheet 6)

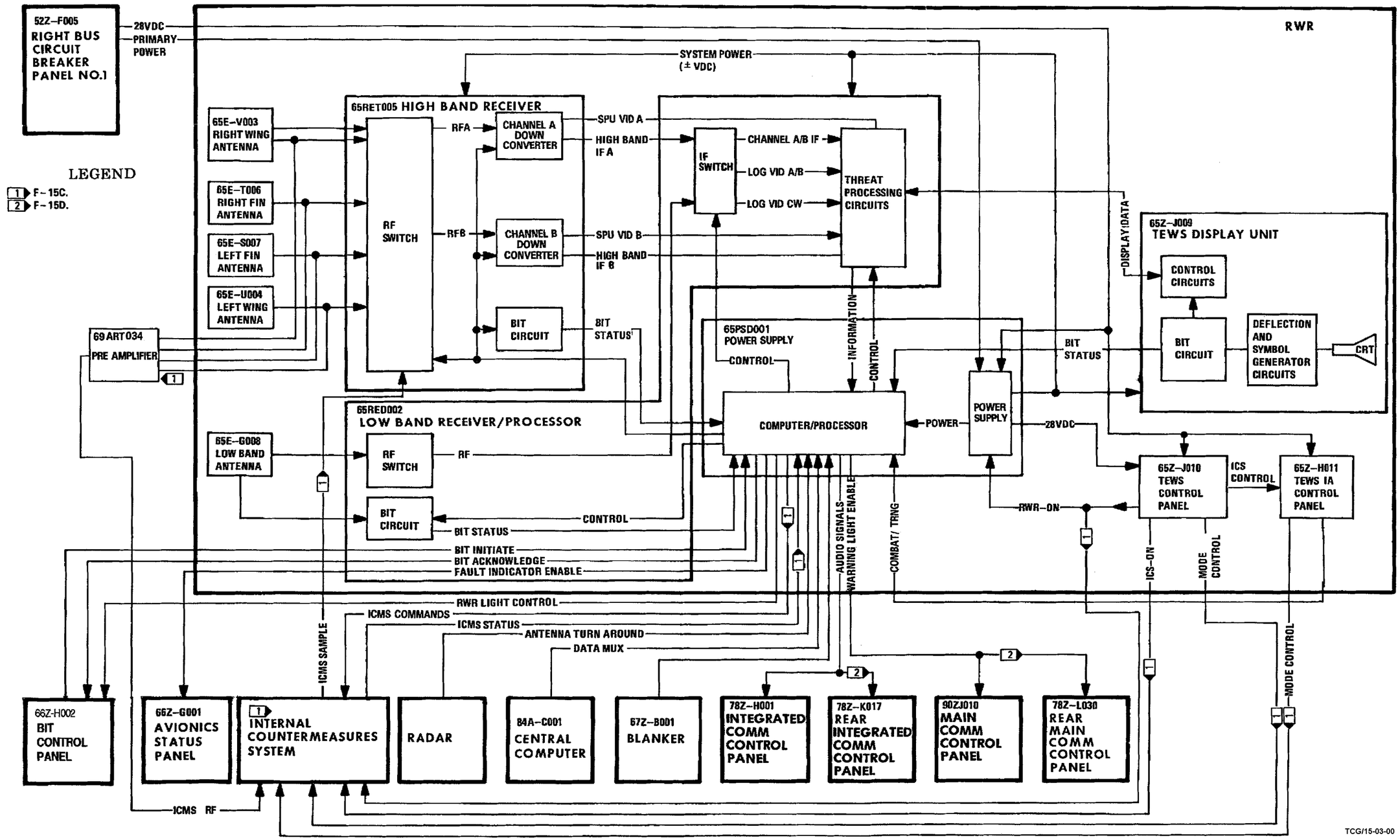


Figure 11-2. RWR Functional Block Diagram

cooling air flow when using external electrical power or single engine operation. The ECS light on caution lights display panel indicates low air flow when on.

11-27. The RWR on signal energizes relay K1 providing fused 3 Ø primary voltage to the power supply module. A 115vac, 400 Hz, Ø A power source is routed to the low band receiver/processor and TEWS display unit to drive their elapsed time indicators. The high band receiver elapsed time indicator uses 28vdc. The 6.3vac, 400 Hz is routed to the TEWS display unit as a display reference voltage. The fused 28vdc is routed to each system LRU fail indicator. The RWR light on the BCP goes out, indicating that power has been applied and the power supply is functional. However, if the power supply fails to turn on, the light remains on. After the RWR has been turned on, the RWR light will come on if there is a system failure.

11-28. The -5vdc, 5vdc, and 15vdc outputs are sent to the high band receiver. The 5vdc output to the low band receiver/processor CPU is remotely sensed. This is to provide voltage regulation at the load for these voltages. At turn-on, all outputs from the DC power supplies are continuously monitored for high voltage, low voltage, or overcurrent conditions. If a malfunction is detected, the power supply and the defective LRU are disabled.

Table 11-2. Controls and Indicators

Control/Indicator	Position/Condition	Function/Indication
TEWS Control Panel		
RWR ON/OFF switch	ON	a. Enables 115vac, 400 hz 3Ø and +28vdc aircraft power application to RWR. b. Applies an RWR ON signal to ICMS, indicating to ICMS that RWR is on and will receive and/or transmit ICMS programmed data.
	OFF	a. Removes RWR system power. b. Disables RWR and ICMS data communication.
1 ▶ ICS ON/OFF switch	ON	Enables 115vac, 400 Hz, 3Ø and +28vdc aircraft power application to ICMS.
	OFF	a. Removes ICMS system power. b. Keeps relay K1, in TEWS control panel, energized, enabling a reduced (10 percent) cooling air application to ICMS.
1 ▶ SET-1, SET-2, SET-3 switches **NOTE:** SET 1= Band 3 SET 2= Band 2 SET 3= Band 1	AUTO	Enables selected ICMS transmitting Set 2 or Set 3 to be controlled by RWR when ICS MAN/AUTO/STBY switch on TEWS IA control panel is in MAN. This switch is non-functional for Set 1 (Band 3).
	MAN	Enables a selected ICMS transmitting set to be controlled independently when ICS MAN/AUTO/ STBY switch on TEWS IA control panel is in MAN.

Table 11-2. Controls and Indicators (CONT.)

Control/Indicator	Position/Condition	Function/Indication
1 ▶ SET-1, SET-2, SET-3 FAIL lights	ON	Indicates a failure in selected ICMS transmitting set.
	Not on	Indicates selected ICMS transmitting set is operating correctly.
1 ▶ EWWS ON/ OFF switch	ON	Not used.
	OFF	Not used.
1 ▶ EWWS TONE/DEFEAT switch	TONE	Not used.
	DEFEAT	Not used.
TEWS IA Control Panel		
RWR/ICS switch	COMBAT	Enables RWR normal preflight message (PFM). Enables ICMS AUTO mode.
	TRNG	Enables RWR training mode and alternate preflight message. Enables ICMS training mode.
1 ▶ PODS XMIT/STBY switch	XMIT	Not used.
	STBY	Not used
1 ▶ ICS MAN/AUTO/STBY switch	MAN	Enables AUTO or MAN modes to be selected by SET-1, 2 or 3 switches on the TEWS control panel.
	AUTO	ICMS sets are maintained in AUTO mode and are controlled by RWR.
	STBY	a. Puts all ICMS sets in STBY mode. b. Keeps relay K1, in TEWS control panel energized, enabling a reduced (10 percent) cooling air application to ICMS.
TEWS Display Unit		
INT control	CW or CCW rotation	Normally controls display intensity. CW rotation increases intensity; however an ambient light photo sensor, mounted on display, automatically adjust display intensity in proportion to ambient light variations.

Table 11-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
BIT Control Panel		
System select switch	RWR	In RWR position selects and tells RWR system when manual BIT is to be done.
INITIATE	Press and release	Enables RWR BIT program.
RWR light	On (steady)	a. When RWR is OFF.
		b. When RWR is on and an RWR system failure occurs.
	On (flashing)	a. Flashes for approximately 10 seconds during time duration of initiated BIT cycle and then goes off.
		b. If light flashes intermittently during normal operation, a partial failure is being detected by program controlled automatic BIT. Receiver operation continues with a possibility of reduced performance.
	Not on	When RWR system is on and operating normally.
Multipurpose Color Display		
Detail BIT display (accessed from BIT 1 display)		
S15 (TEWS)	Press and release	Enables TEWS detail bit display.
TEWS detail BIT display (accessed from detail BIT display)		
S4 (ICS BIT LOG)	Press and release	Enable ICS BIT log display.
S6 (RWR)	Press and release	Enables RWR functional fault display.
S7 (ICS)	Press and release	Enables ICMS functional fault display.
RWR detail BIT display (accessed from TEWS detail BIT display)		
S6 (RWR)	Press and release	a. Will be displayed in the RWR detail BIT display to indicate RWR detail BIT data is being provided.
		b. When pressed from the RWR detail BIT, display will return to the TEWS detail BIT display.
S11 (MENU)	Press and release	Returns to menu 1 display.
S15 (TEWS)	Press and release	Returns to the TEWS detail BIT display.
BIT	Displayed	Indicates the system is in a BIT display.

Table 11-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
NO DATA AVAILABLE	Displayed	Indicates that CC recognizes a previous software version.
NO RWR/CC 1553 COM	Displayed	Indicates there is no RWR/CC communication the 1553 data bus, or that there is communication on the H009 data bus.
* Functional Failure #	Displayed	An asterisk * to the left of the functional failure message indicates a frequency degradation associated with the failure message. The frequency range affected is specified at the bottom of the display.
TEWS display (accessed from menu 1)		
S14	Press and release	Scrolls between combat PFM legends.
Integrated Communication Control Panel		
TEWS LAUNCH DISABLE switch	Press and release	Disables launch tone.
TEWS LAUNCH AUDIO volume control	CW or CCW rotation	Adjust volume of launch (modulated) tone.
TEWS CAUTION AUDIO volume control	CW or CCW rotation	Adjusts volume of caution (steady) tone.
Main Comm Control Panel		
AI light	On	Classified secret. Refer to TO SR1F-15C-2-99GS-00-2, section 11.
SAM light	On	Classified secret. Refer to TO SR1F-15C-99GS-00-2, section 11
1 ▶ Not related to RWR operation.		

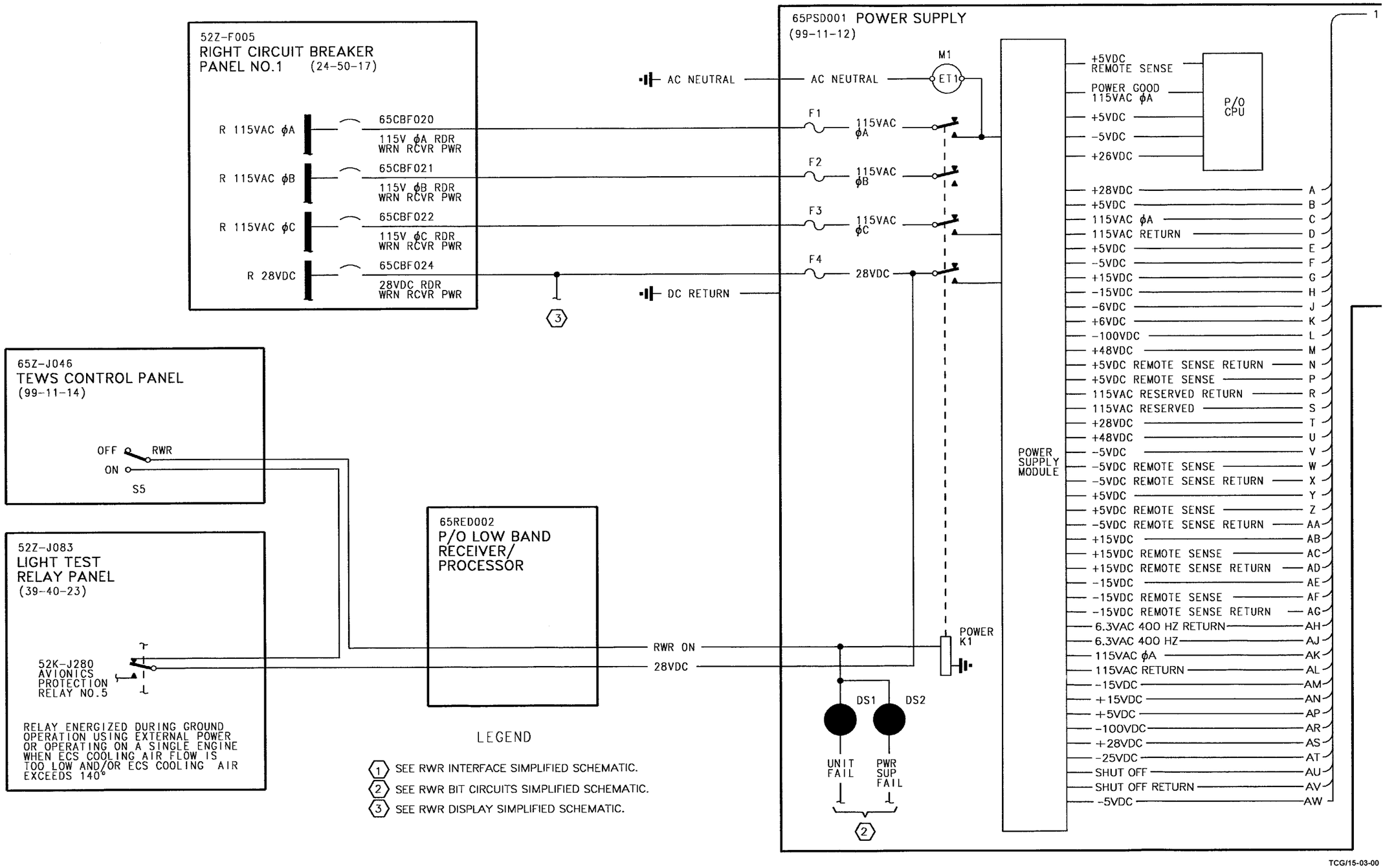


Figure 11-3. RWR Power Distribution Simplified Schematic (Sheet 1 of 3)

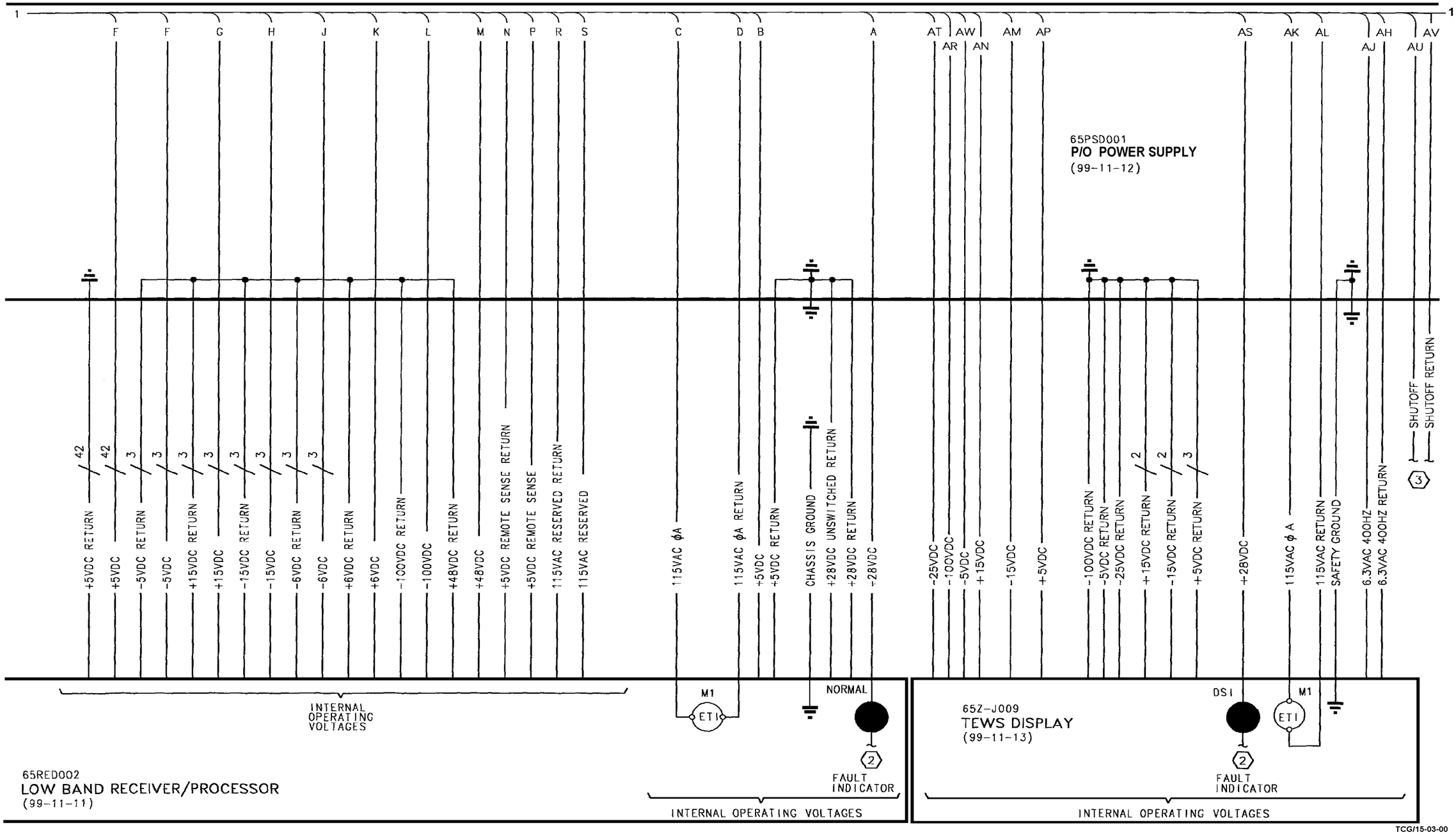


Figure 11-3. RWR Power Distribution Simplified Schematic (Sheet 2)

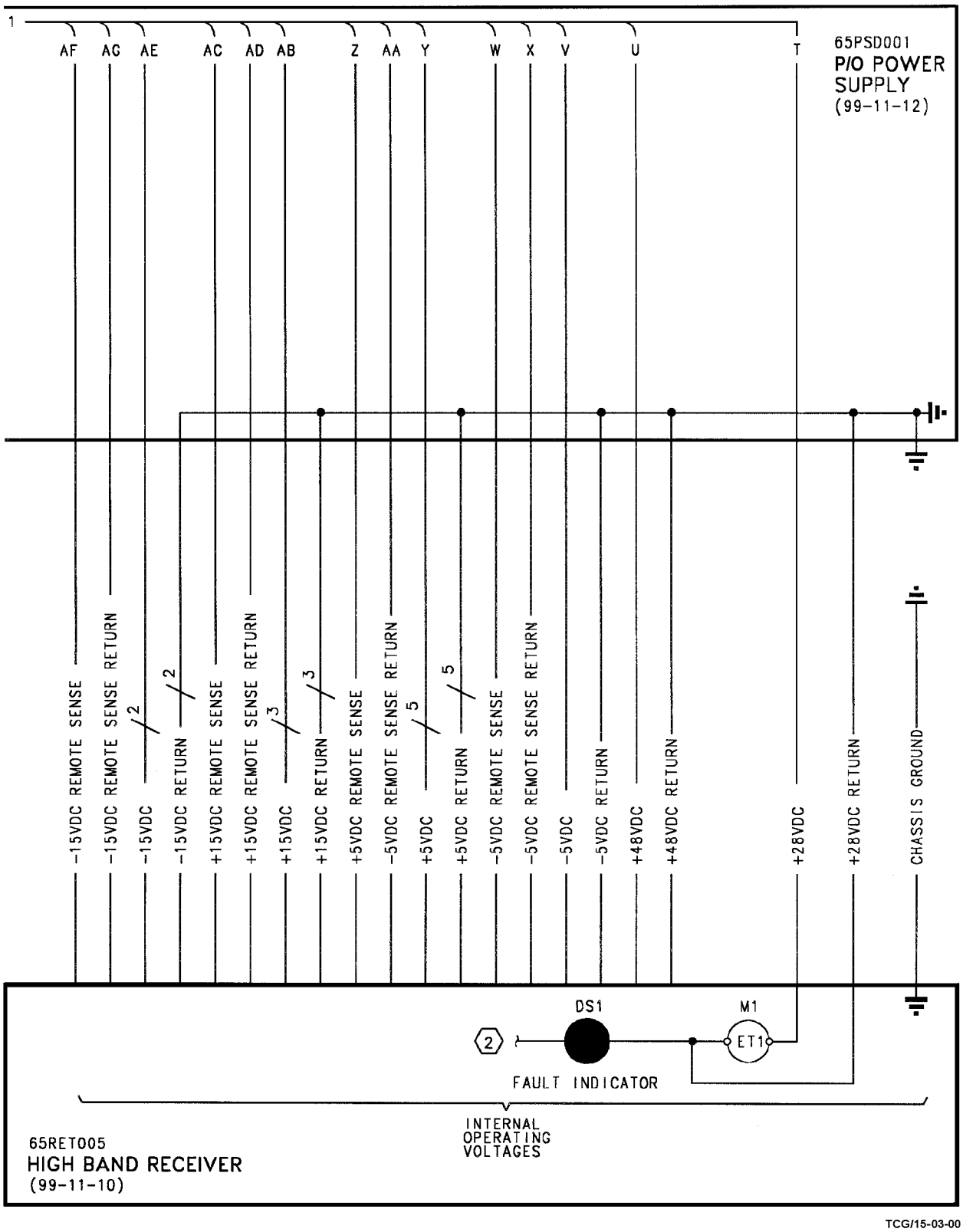
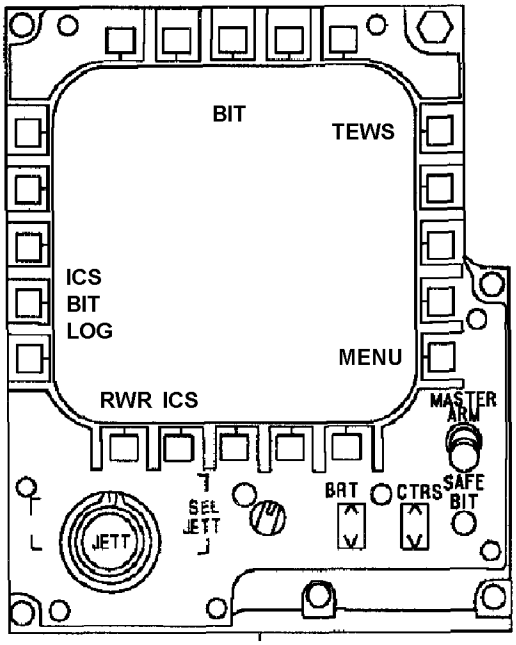
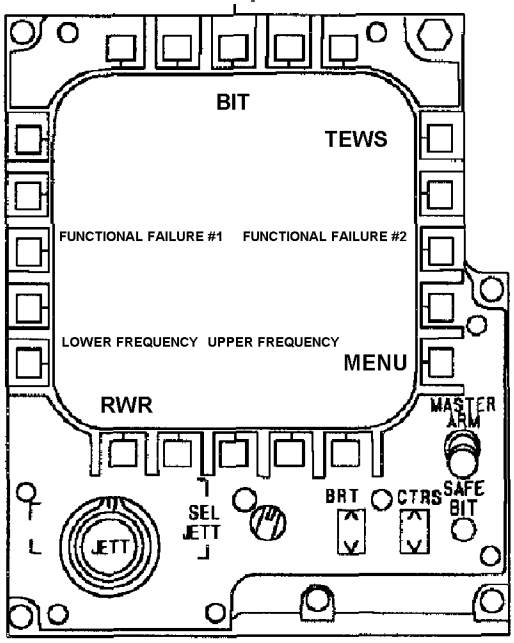


Figure 11-3. RWR Power Distribution Simplified Schematic (Sheet 3)

DETAIL BIT DISPLAY





RWR DETAIL BIT DISPLAY

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Figure 11-4. RWR Displays

11-29. **Receiving Circuits** See Figure 11-5.

11-30. **High Band Signal Acquisition.** High band signal acquisition is done by the high band receiver and four antennas with a RF sample from the jammer. Processing of the incoming RF signals is controlled by receiver control signals applied in serial format from the computer/processor. This input data is received as a serial manchester coded word, allowing both data and clock signals to be transmitted on a single transmission line. Receiver control selects the RF switches and antennas, frequency band, receiver tuning, attenuation, and BIT during high band receiver operation.

11-31. After computer/processor initialization, the computer/processor transmits a receiver data signal which is applied to the input data control. The computer-demand and computer command address signals enable the data to be manchester coded. The received data is applied to a shift register and manchester decoder. The manchester decoder and clock generator decode the control instruction word and produce the clock frequency. The clock is used to shift the control instruction word out of the register to the address decoder and the various control latches in the receiver. The clock is also used for sychronization. and timing.

11-32. Signals in the high band frequency range are intercepted by four antennas; the right and left wing antenna and the right and left fin antenna. The right wing antenna has a down looking element for elevation coverage. The antenna inputs along with ICMS summing RF BIT oscillator inputs are applied to RF switches. Each antenna provides 90 degrees of coverage. Together, through switching, the signals provide omni coverage. During direction finding (DF) analysis, switch separation of the RF signals provide direction finding abilities.

11-33. The high band receiver amplifies high band antenna signals and converts these signals to the intermediate frequency. There are two separate channels (Channel A and Channel B) that deliver two IF and two SPU video output signals. Also, the low-band frequency range is up-converted to be processed in the same manner as the antenna signals.

11-34. The RF signals from the four antennas are applied to Channel A and B RF switches; where the antenna input signals are selected and switched. In normal mode, one antenna signal is fed to Channel B, and one to Channel A to provide two simultaneous IF output signals. The four antenna inputs may also be selected in any combination up to 50 nanoseconds after which time a new combination is selected for the next 50 nanoseconds. The cycle would then repeat continuously. Scanning may include the entire frequency range, or any number of segments in this range. The computer/processor controls the scan by generating digital signals which are applied to the low band receiver/processor Channel A and B in parallel. The Band II down converts in each channel converting the signals to Band I frequency range. The Band I signals are again down converted to IF signals. By power splitting the RF signal, SPU signals are developed.

11-35. **Low Band Signal Acquisition.** When there is a low band signal to be processed, the Chan A/low band RF is applied to the IF/low band switch of Channel A. The Chan A/low band sign IF is raised to a Band I frequency by mixing with a local oscillator signal. From this point, the IF and SPU video signals are developed for the Chan A/low band IF in the same manner as for the antenna input signals; except, only Channel B outputs are used, since Channel A is occupied with the Chan A/low band IF input from the low band receiver/processor.

11-36. BIT operating and calibration makes use of the harmonic generator and noise generator. The harmonic generator is used for calibration of the local oscillator and for digital delay calibration. It is also used as an input test signals to measure the difference between Channel B and Channel A gain (Channel unbalance). The noise generator provides a known excess noise level (power-frequency spectrum) to test average receiver gain over the IF bandpass of 500 MHz.

11-37. **IF Processing.** Each IF Channel has switches, filters, and amplifiers for bandwidth control and signal compression (logging). The receiver control signal sets the switches for the selected mode. Both channels operate symmetrically; so that, when a particular path is enabled in one, the same path is enabled in the other (with the exception of low band and BIT). There are four such modes that operate symmetrically: wide band, medium band, notch and CW.

11-38. In wideband, the full IF bandwidth from the high-band receiver is passed unfiltered. In medium band, the IF bandwidth is limited by an A and B filter. The notch filter is enabled when there is an undesired frequency anywhere in the bandwidth. In CW mode, the IF signal is steered to the channel sel for CW

filtering. The CW channel has two operating modes plus BIT. The two modes are CW coarse and CW fine. In CW coarse, the CW IF bandwidth is limited by CW channel sel. Since there is only one CW coarse filter, both channels are looked at sequentially. This is done by a commutating switch. In CW fine, the IF signal coming through the CW channel sel is distributed through a power divider. One output of the power divider is superheterodyned down in fine gain, so it falls within the bandpass of a very narrow-band surface acoustic wave (SAW) filter. The filter in conjunction with the VCO and a mixer allows for detection of multiple CW signals. The SAW mode operates only in high band. The CW coarse output of the power divider is fed directly to coarse/fine CW switch. The selected frequency (coarse or fine) is detected and amplified to produce LOG VID CW.

11-39. During BIT operation, LO (local oscillator) is used for a superheterodyned BIT source. The BIT source is used for low band antenna receiver and IF/ processor testing. The C/D band switch selects the signal from the low band antenna when low band mode is enabled, low band noise, or the local oscillator when BIT is required. The selected signal is amplified and sent back through channel A switching, to the high band receiver for up-conversion.

11-40. In wide and medium band, the channelizer is used to select one channel at a time. The channel with the greater amplitude is selected by the rec control signal from the computer/processor. The limiter receives the delayed signal and outputs a constant power range of input power. In the channelizer, power dividers distribute the signal simultaneously to 13 bandpass filters. A detector follows each filter and the resulting video signals identify the IF frequency.

11-41. **Computer/Processor Unit.** The computer/ processor, located in the power supply, is a digital computer which meets all the high-speed mathematical processing requirements of the RWR. The computer/ processor is made up of three major sections as listed below:

a. P BUS interface

b. DMA interface

c. Processor (CPU)

A simplified diagram of the computer/processor is shown in Figure 11-6.

11-42. **P BUS Interface.** The P BUS interface provides one parallel to serial output channel, one serial to parallel input channel, and the necessary protocol discrete inputs. The input channel, the output channel and controllers operate at a 5 megahertz rate. All command address words and demands for service originate at the processor. Control signals are passed on to the DMA interface after clearing and turning on all channels (initialization), the P BUS interface waits for a service demand from the processor. The processor can issue any of 11 commands. These include four DMA channel clears, four DMA channel enables, system reset, input or output P BUS data and load status data. When the processor commands the clearing or enabling of a DMA channel, the appropriate clear DMA signal or turn-on DMA signal is sent and receipt of the command is acknowledged. When the processor requests to output data, the P BUS interface tests the register full flag. If it is inactive, the data is loaded into the register and acknowledges receipt of the command. When the processor requests to input data, the P BUS interface tests to see if the register is full. If so, it outputs the data, acknowledges the command and clears. The interrupts from the low band receiver/ processor are applied to the P BUS interface.

11-43. **DMA Interface.** The DMA interface provides three serial-to-parallel input channels, a parallel-to-serial output channel, and the necessary handshake protocols. The controllers and channels operate at a 5 megahertz rate. Control signals for the clearing of channels, the enabling of channels, and rebound testing are provided from the P BUS interface. The four channels of the DMA interface are initialized by enabling and clearing signals from the P BUS interface. Then, while waiting for the register to be filled with DMA input data from any one of the three input channels, the DMA CPU interface demands a DMA output from the processor. When any such input occurs, the DMA CPU interface immediately demands input service from the processor. Any refusal of service from the processor concerning a specific channel causes the DMA interface to disable the channel. The only way to re-enable the channel is by signal from the P BUS interface. When a full signal from any of the three input channels exists, the applicable register full flag is set. If two channels are simultaneously full, the state control firmware in the DMA interface establishes service priority. Any full input channel outputs a busy signal to the low band receiver/processor until it is serialized and cleared. When a full indication is sensed, the channel is enabled and it outputs a demand to the processor. Either a no-acknowledge or an acknowledge is received. The interface then either turns off the channel or outputs the data. The register full flag is

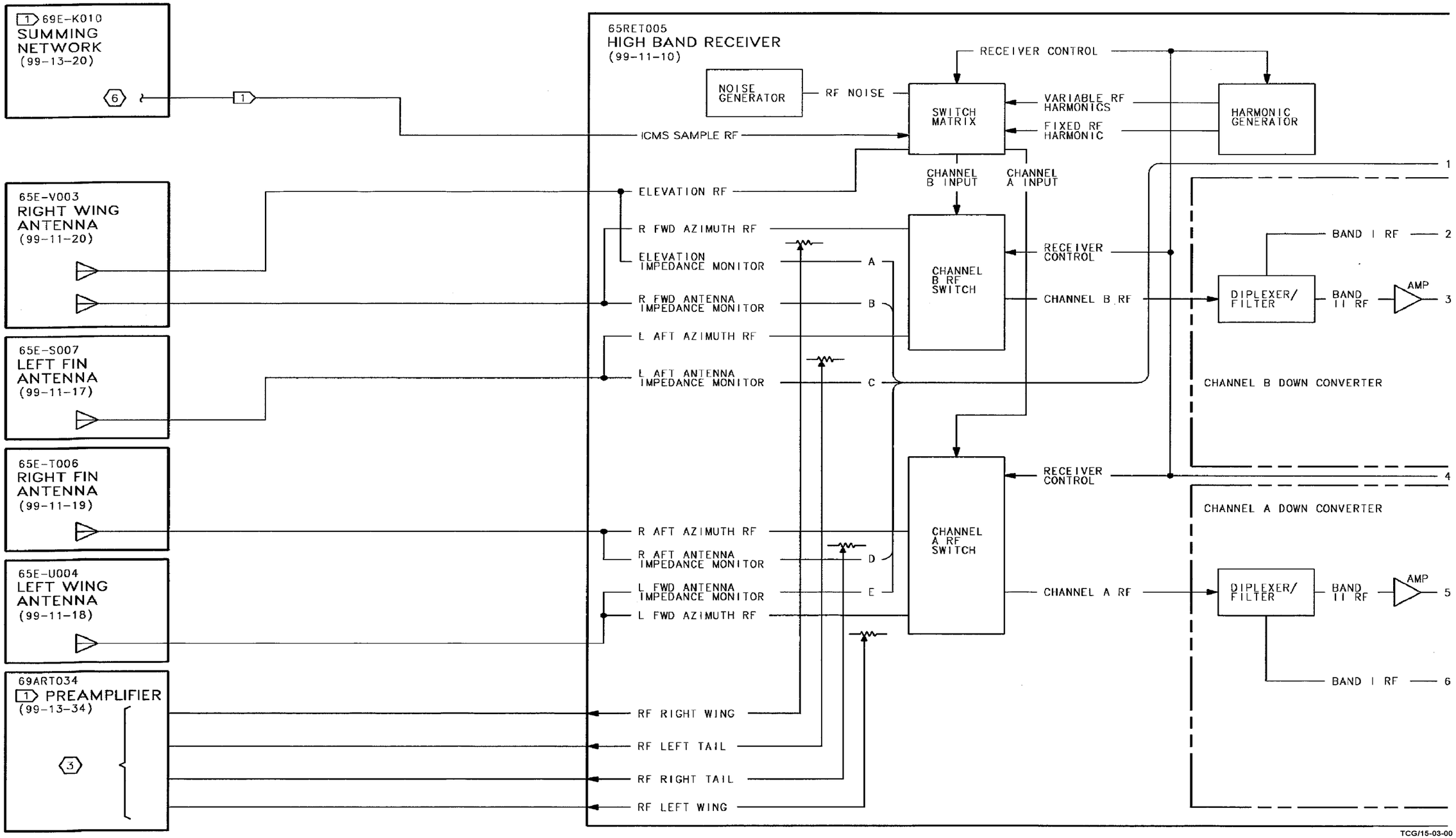


Figure 11-5. RWR Receiving Simplified Schematic (Sheet 1 of 3)

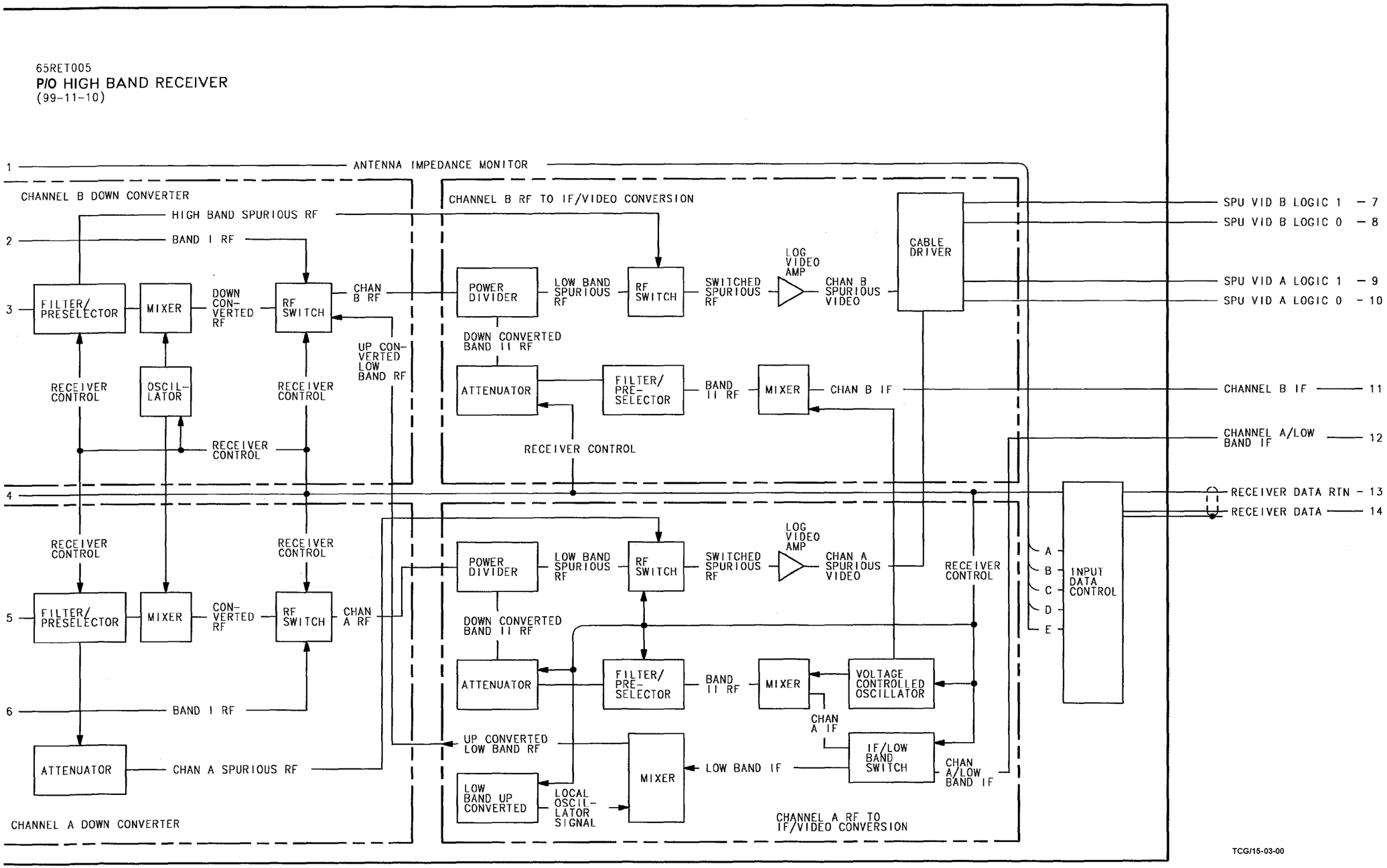


Figure 11-5. RWR Receiving Simplified Schematic (Sheet 2)

LEGEND

FAULT INDICATORS
(BLACK AND WHITE)

(FAILED POSITION SHOWN)

1 F-15C
2 SEE RWR POWER DISTRIBUTION SIMPLIFIED SCHEMATIC.
3 SEE RWR INTERFACE SIMPLIFIED SCHEMATIC.
4 SEE RWR THREAT PROCESSING SIMPLIFIED SCHEMATIC.
5 SEE RWR BIT CIRCUIT SIMPLIFIED SCHEMATIC.
6 SEE ICMS INTERFACE SIMPLIFIED SCHEMATIC.

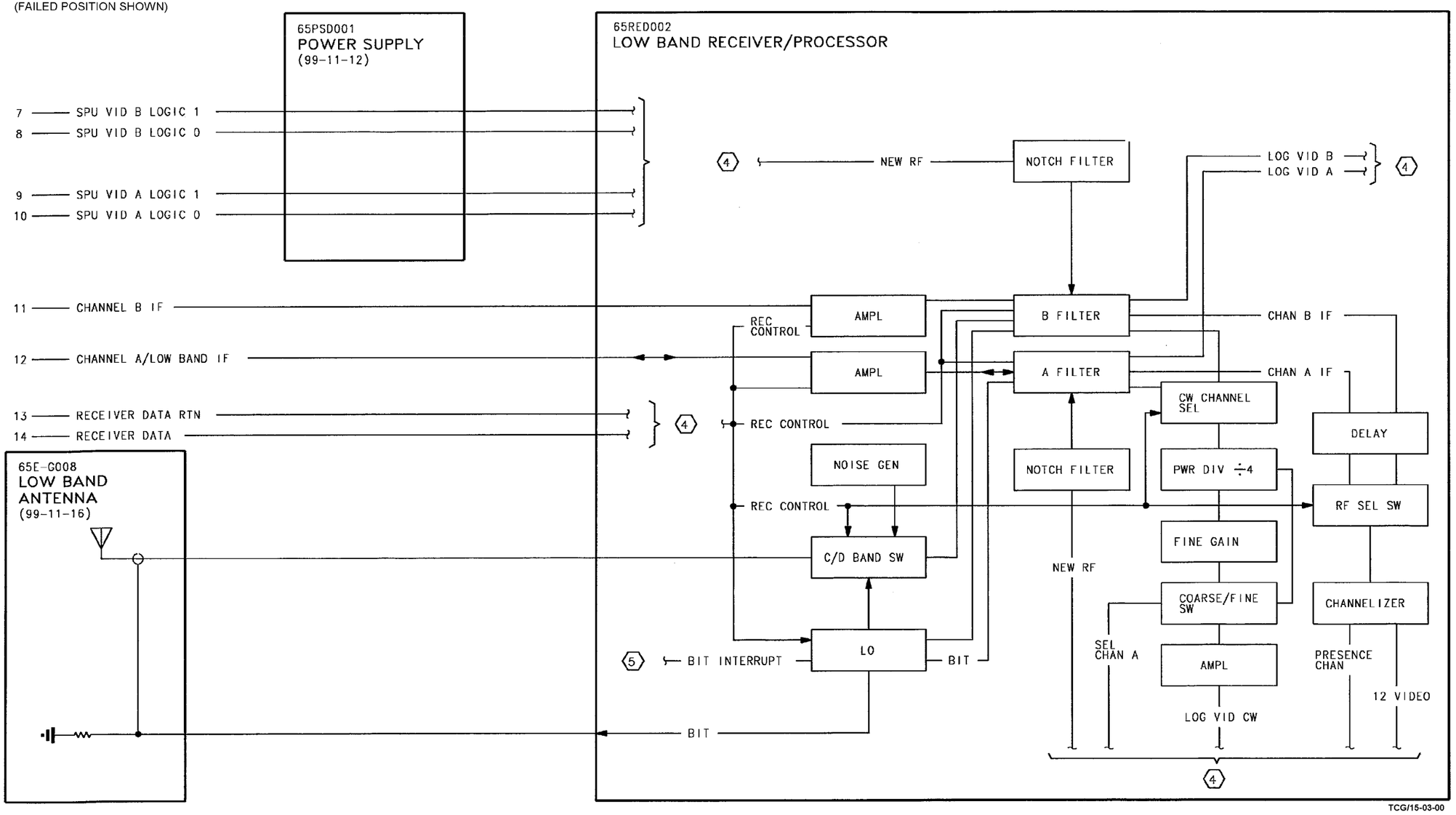
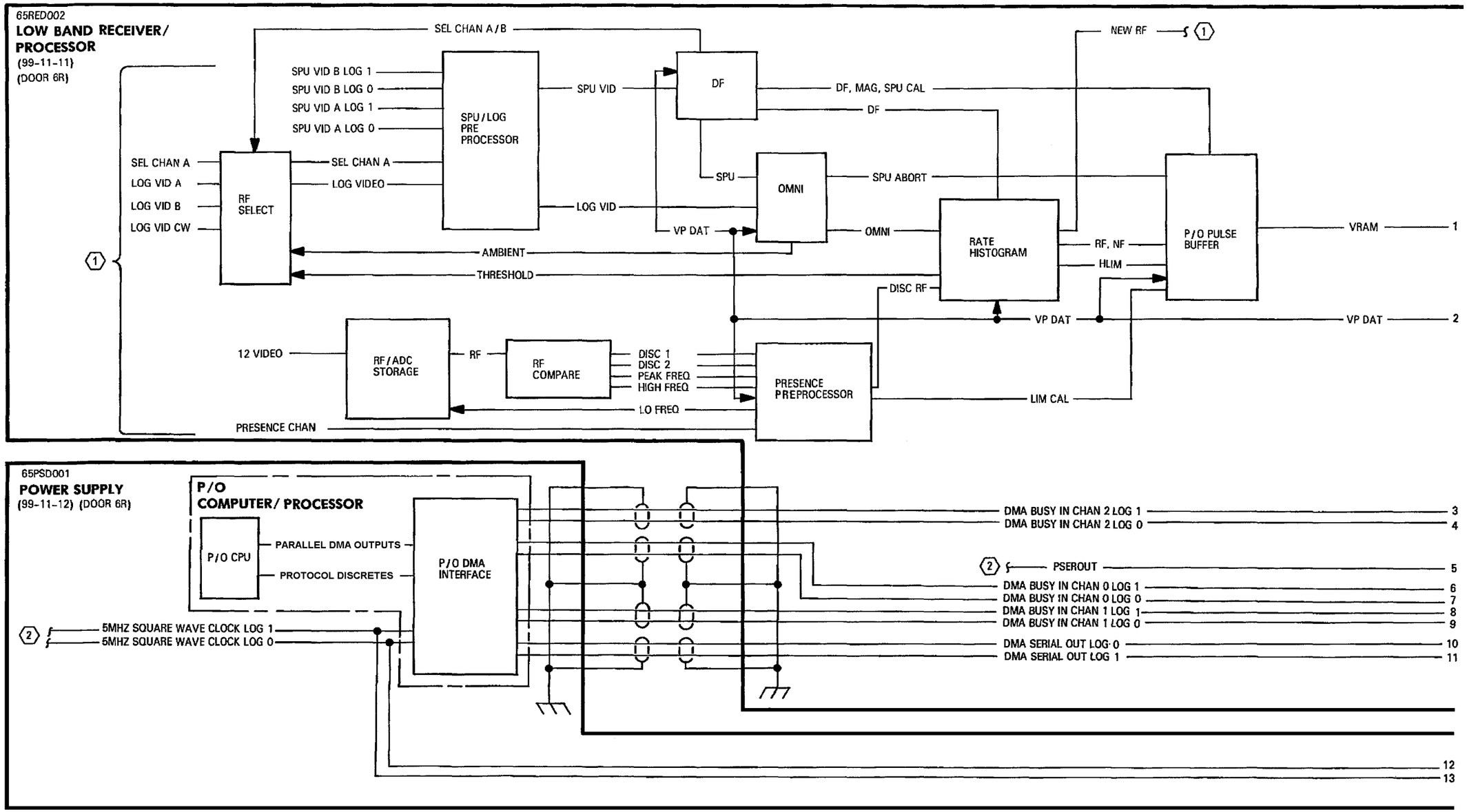


Figure 11-5. RWR Receiving Simplified Schematic (Sheet 3)



LEGEND

(1) SEE RWR RECEIVING SIMPLIFIED SCHEMATIC
(2) SEE RWR INTERFACE SIMPLIFIED SCHEMATIC
(3) SEE RWR BIT SIMPLIFIED SCHEMATIC

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Figure 11-6. RWR Threat Processing Simplified Schematic (Sheet 1 of 3)

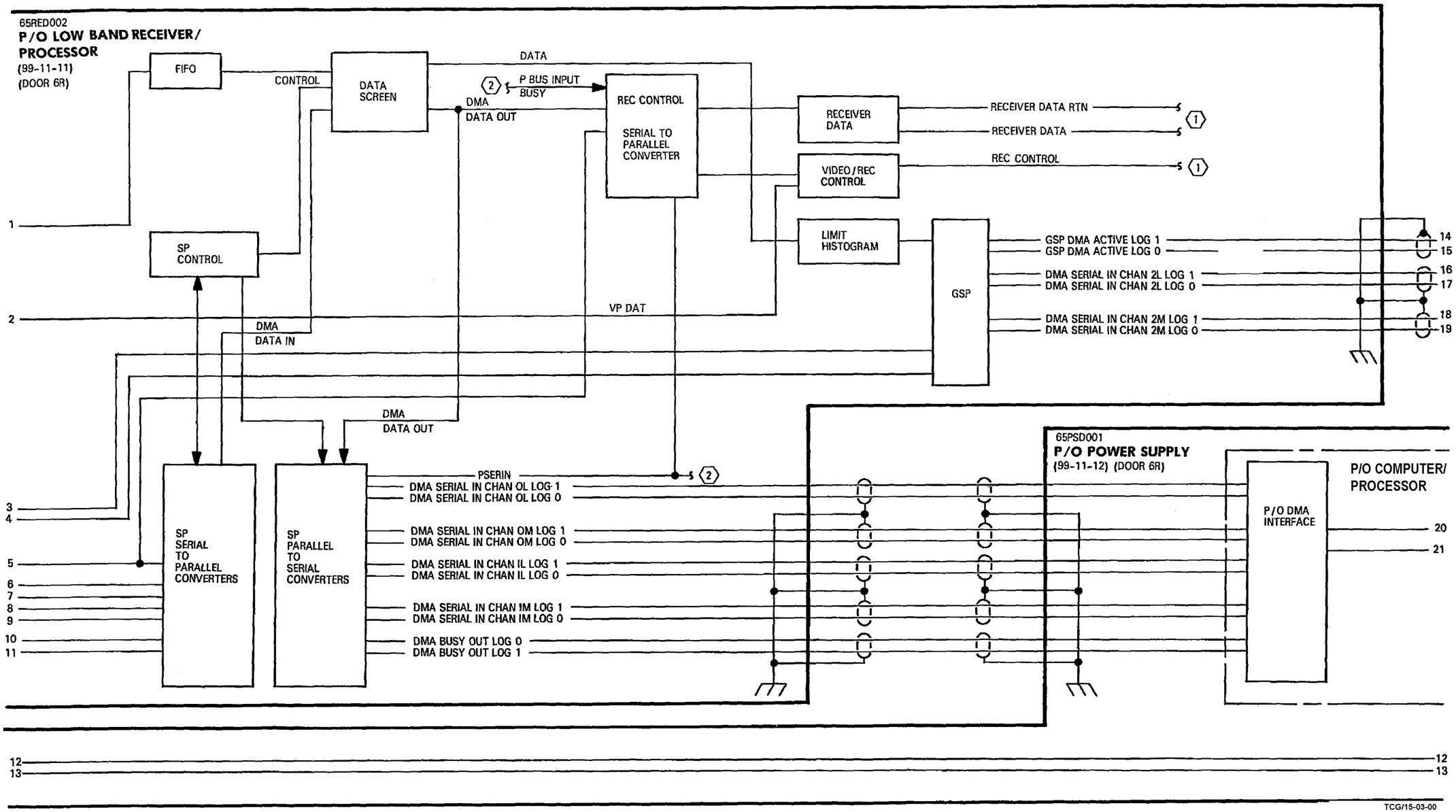


Figure 11-6. RWR Threat Processing Simplified Schematic (Sheet 2)

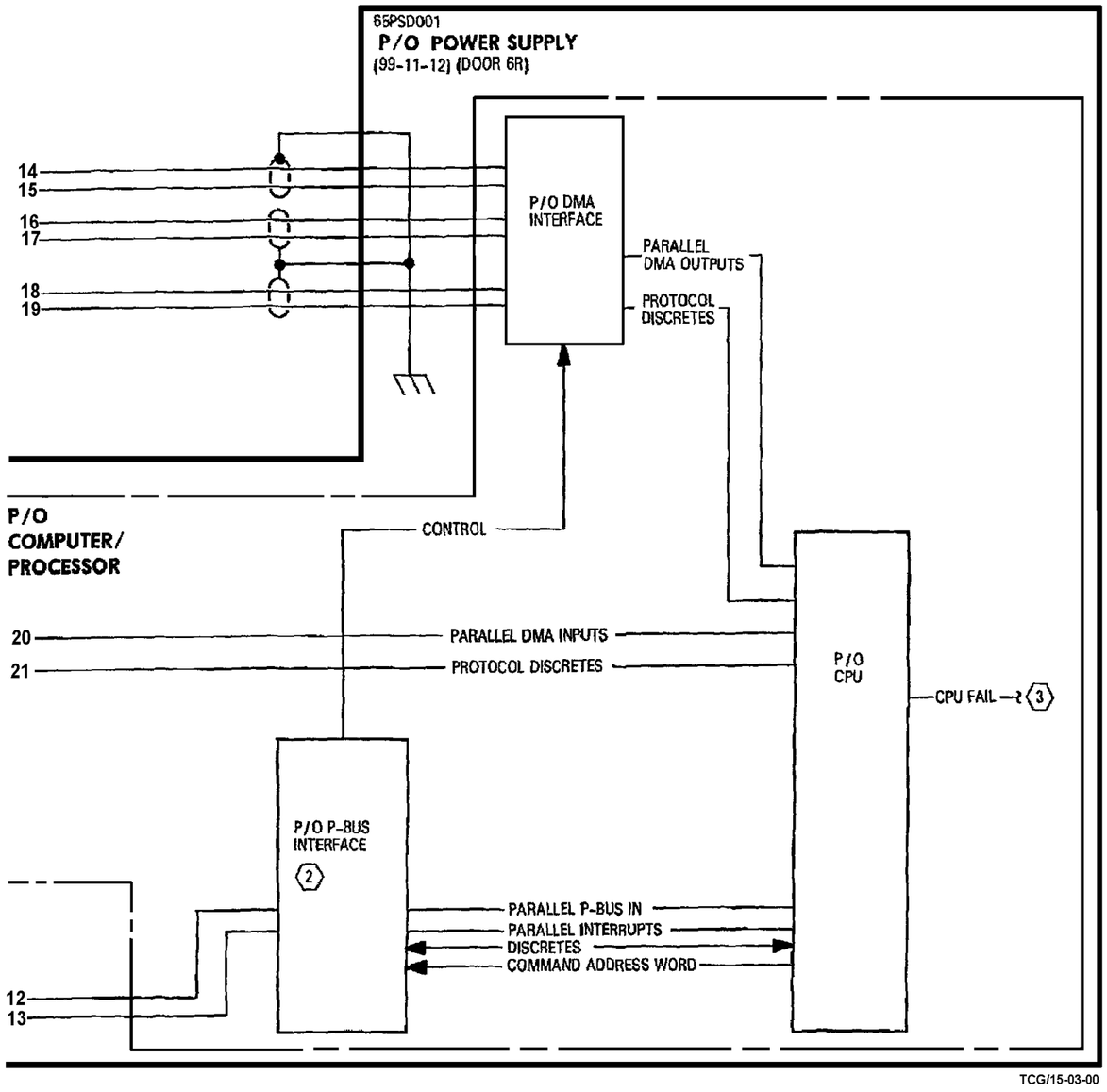


Figure 11-6. RWR Threat Processing Simplified Schematic (Sheet 3)

cleared. When full flag is set and the channel is enabled, the interface test the DMA busy to determine if data can be sent. If any channel is running rebound tests, the DMA busy is not tested and the data is immediately shifted out. If no rebound test is in progress and busy is not active, the data is shifted out and the full flag is cleared. This allows the interface to load data again when the data is ready from the processor.

11-44. **Processor.** The processor provides the data paths, registers, arithmetic unit, and various other logic required to do the data handling specified by the program instruction being executed. The processor keeps track of the instruction being executed, provides temporary storage for the instruction word loaded from program memory, does all arithmetic, logical and shift and compare operations required for execution of program instructions. A 16-bit by 16-bit general register is used for temporary storage of primary operand, results of previous instructions, and input/ output data. Selection of one of the sixteen 16-bit registers is controlled by a selected field of the instruction word. The output of the register file is applied to multiplexers. This permits parallel operations within the general register file and removes the requirements of storing intermediate values in temporary memory locations.

11-45. Computer memory is addressed in 4K blocks. Successive addresses are compared to previous addresses in holding register. This reduces memory access time. The processor has the ability of directly accessing 256K words of the memory paging scheme. The processor handles the P BUS interface processing. The direct memory access controller provides data transfers between the computer memory and the low band receiver/processor on the DMA interface.

11-46. **THREAT PROCESSING CIRCUITS.** See Figure 11-6.

11-47. **High Band and Low Band Threat Processing.** Threat processing of the high and low band IF signals is completed by the threat processing circuits in the low band receiver/processor. The log video signals are tested for a lim video presence to determine if the radar signal exists in the IF bandpass and the channel receiving the strongest signal. Then, the pulse width of the log video signal selected for analysis is measured and tested against PFM limits. If the pulse width of the received signal is within limits, the time of arrival of each such confirmed pulse is measured. The signal is then compared together with the fine frequency data of the discriminator and the signal amplitude. If a radar pulse is not received, the processing continues for one pulse-repetition-interval (PRI) at the same RF segment. If a radar pulse is received, the processing is continued for a minimum of four intervals. Several determinations are made using the time of arrival data, these are: (1) if more than one radar signal is present. (2) the PRI of each radar signal. (3) the presence of a staggered PRI (4) the presence of agile PRI signal. If the analysis of the PRI is correct as compared to the PFM, those PRI which match threat radar characteristics are further analyzed for other threat parameters and stored. Direction-finding measurements are done on any high band signal identified as a threat. Guidance correlation is done on any SAM guidance radar detected in the low-band frequency range.

11-48. RF select converts the log video data (Channel A, Channel B, and CW) into six-bit digital format. The data is sent to the SPU/log preprocessor. The IF select detects a 6 db use in any channel with respect to either channels two antennas and freezes ambient if the signal is also above threshold. Ambient remains frozen until a command is received to unfreeze the ambient and the SPU/log preprocessor accepts the digitized video data and outputs four sets (channels) of log video data. Each channel output is the maximum of the two samples accepted by that channel in each 200-nanosecond frame. Each channel carries six bits of log video data. One bit indicates the frame half in which the maximum of the two samples occurred. One bit indicates the position of the switch during that sample interval. The SPU/preprocessor converts Channel A and Channel B SPU video, and outputs digitized six-bit video data. Each sample corresponds to the selected log video sample on a frame-by-frame basis. The omni board accepts the log video data. Each incoming video sample is compared to the current threshold. The current signal level for each of the four sets of data are continuously stored for establishing a running ambience. Ambience refers to the video amplitude level two frames before the pulse leading edge. The term channel used in this discussion refers to one of four sets of data of the SPU/LOG preprocessor. The greater of channels 0 and 2, and channels 1 and 3 are determined on a frame-by-frame basis. An omni peak is detected as one of the four channels whose amplitude exceeds threshold and is at least 6 db above its own ambience and whose amplitude is greater than that of

any of the other three channels. All amplitudes are with respect to the ambience of the respective channel. The DF peak is measured in a manner similar to that of the omni peak. The candidate for the DF peak is not required to be at least 6 db greater than ambience. The highest values are outputted as candidates for DF peak and omni peak. A comparison is made of omni peak and SPU to determine validity of the pulse. If SPU is too high, signal SPU ABORT is transmitted.

11-49. The DF computes the DF peak of each DF candidate over a three frame interval and then selects the maximum DF of the two DF peak candidates. The DF stores ambient samples and converts the leveling value for ambience. The converted video is available for output to the computer/processor in the SPU calibration mode. A look-up table accounts for the difference in cable losses from the two antennas used in the DF computation. The look-up table also provides magnitude change as a function of DF ratio. The DF is applied to the rate histogram. The rate histogram provides rate histogramming and rate limits for pulse parameters. The rate histogram tunes the IF notch filter and shifts threshold on signals that reach a magnitude limit. The rate histogram responds to computer/ processor commands to provide eight selectable CW activity histograms. The rate histogram subjects each pulse to various histogram algorithms whose limits are partially controlled by the computer/processor to establish rejection criteria. The pulse buffer serves as the interface storage element for the FIFO (first in first out). The pulse buffer holds data while the rate histogram determines if the data should be passed or not.

11-50. The RF/ADC storage provides bulk storage for RF video samples for subsequent use in determining the pulse RF. The RF video sample from each of the 12 channelizer outputs is stored in a 32 X 6 RF memory. This memory serves as a programmed delay line to account for the offset that exists between an RF sample and the omni peak antenna identification at leveling. The output of the RF/ADC storage are 12 detected outputs, each represents a specific 50 MHz region of the 500 MHz IF. Additional 50 MHz are added on the two ends of the 500 MHz IF for the purpose of discriminator measurement and guard band protection. The RF compare computes the delta RF, or RF deviation from filter center by noting the relative value of the two global peak adjacent channel amplitudes and the peak global peak channel amplitude. If the differences between the remote adjacent and the threshold is positive, it signifies a larger amplitude from the remote adjacent channel that would be expected for a single RF signal. The RF comparator computes the RF of the signal. The presence preprocessor converts the presence video and stores the samples in a 32 X 8 RF memory. The selected RF sample is compared to an established limiter threshold (VP DAT). The output of the presence preprocessor is LIM CAL. The presence preprocessor stores the 64 correction values for wide band mode and discriminator readings for narrow-band mode. The correction and discriminator outputs are applied to the rate histogram to maintain channel balance. The pulse data from the pulse buffer is loaded into a FIFO which acts as temporary storage. Pulse data read out of the FIFO is subjected to the screen filter test.

11-51. Prior to each receiver dwell, the computer/ processor loads a set of screening parameters. DMA data in is made up of the upper and lower acceptance limits of RF, DF, PW, and amplitude threshold. These values define an acceptance or rejection window for all collected data. Up to eight sets of screens may be loaded for each receiver dwell. When a pulse meets all the above requirements, it is handled in accordance with the control flags previously loaded by the computer/processor. The pulse data is routed to both the GSP (group statement processor) and the computer/ processor. The pulse is also directed to the histogram limit test before being set to the computer/processor or to the GSP. Pulses that do not correlate with any window are sent to the GSP subject to passing the limit histogram criteria. The limit histogram stores the count of pulses from all emitters in applicable cells or bins containing; stable RF and DF pulses, pulses occurring during overfly, and agile RF pulses. When a pulse occurs, the DF counts associated with the pulse are examined. If the DF count is 15 and the new DF count is seven, an agile RF exists at this DF. If the RF count is less than four, then it indicates that there is not an RF stable signal existing at this RF and DF. This is true because we assume that RF agile families have their frequencies spread out and will not repeat. Thus, RF stables are separated from RF agiles by examining the RF count and making sure that it is small. The GSP is a special purpose digital processor which allows a special series of algorithms. The GSP isolates all the pulses belonging to each emitter from pulse data containing multiple emitters. The GSP sorts and identifies all pulses that belong to a unique emitter and provide the computer/processor with descriptors

describing the groups behavior of the pulses that have been tagged as belonging to the unique emitters. The GSP now provides the computer/processor with digital descriptors of the pulse group behavior characteristics that are the signatures of the input signals. The group statements show the computer/processor singular RF, DF, pulse width, and PPI descriptors of the group behavior of all pulses from this single train that has been illuminating the aircraft.

11-52. The computer/processor examines the group statement data content and decides whether the information is valid and a threat exists. If so, it schedules further analysis of that particular RF area of space which contained the input signal. Additional analysis is made to determine the scan period, launch status and associability of the particular emitter with an already acquired beam stored in the threat history of the computer/processor memory. This additional scheduled analysis is done by tuning the receiver to the group statement frequency description, collecting, and analyzing the individual pulse data directly. When the pulse data proves that the emitter is a threat, subsequent updates of the particular emitter parameters will be done.

11-53. The functions of the rec control are to tune the high band receiver and control the IF in the low band receiver/processor. When the rec control gets receiver data from the computer/processor, it is transmitted to the high band receiver as receiver data. This data is stored until the receiver data transmits a command word to the high band receiver to retune. At the same time the high band receiver is receiving tuning data, the video rec control is storing DMA OUT and PSEROUT data in the tuning data ram. The signals from the RAM, REC Control and VP DAT signals, control the IF circuits in the low band receiver/processor.

11-54. **DISPLAY CIRCUITS.** See Figure 11-7. The TEWS display unit usually displays the priority threat symbols in range, position, and intensity as determined by threat processing. The PDATO signal from the signal interface, when decoded, supplies the control word address for each data transmission and the control instruction data of each transmission, controls X and Y deflection, character and symbol production, and intensity modulation. The clock gen/display store controls the output data to the manchester encoder or BIT and shut down during a power reset. A data req will produce a data out request. The data out request is combined within the interface input with other CPU signals and a PSERIN signal is sent to the RWR interface.

11-55. The received data is Manchester decoded and stored in four shift registers: the X and Y position registers, character register, and instruction code register. The Manchester decoder also produces a 1 MHz clock. The 1 MHz clock is NAND'ed with DATA REQ to produce the shift register clock. The 1 MHz clock is also divided down to produce various timing clocks. The character register contents are loaded into the address counter to select the part of the display unit internal program which produces the selected character/symbol. The instruction code register determines if the character/symbol is to be enclosed in a circle, is to be intensified, or is to blink on and off. The outputs of the X and Y registers are applied to the X and Y D/A converter, and its analog voltage output indicates the position of the alphanumeric symbol on the CRT.

11-56. The addressable programmable read only memory (PROM) contains the program for character/ symbol production, turning on the CRT and display unit self test. A timing signal enables the character/ symbol data to be applied to the address counter and control multiplexer. The address counter output signal sequentially addresses the PROM. On being addressed the PROM provides the control instruction signals to produce that specific character/symbol. Also, PROM control instruction signals are applied to the control multiplexer and, when enabled by the SYNC signal (66.6 Hz refresh rate), produce control signals that enable the PROM control instruction signals to be applied to the stroke generator, phosphor protector, and Z-axis amplifier. The 66.6 Hz sync signal is derived by dividing a 400 Hz clock signal developed by the phosphor protector. This 400 Hz clock signal is derived by synchronizing a 6.3vac reference voltage from the power supply. If the 6.3vac is not available, a display fail occurs.

11-57. In the Stroke Generator the character/symbol control instruction signals are integrated with a ±vdc stroke reference level to produce X and Y ramp voltages. The X and Y ramp voltages are summed with the X and Y analog position voltages, and the summed output X and Y composite stroke (symbol and position) analog voltages are then applied to the Phosphor Protector.

11-58. Phosphor Protector works as a unity gain voltage amplifier for all stroke and position voltages.

However, during range/bearing dot production the stroke and position voltages are scaled for a higher gain. The output voltages (X scaled and Y scaled) are applied to X and Y preamplifier.

11-59. The X-Y Preamplifier, Yoke Drive Assembly, and the Deflection Yoke operate as a single unit. The preamplifiers and high gain amplifiers receive the X and Y scaled voltages and apply them to the yoke drive assembly. The yoke drive assembly, effectively a current amplifier, applies its output signals LX and LY to the deflection yoke, positioning the character and/or symbol on the CRT. The deflection yoke feedback signals LXRTN and LYRTN help control the total gain.

11-60. When characters and/or symbols are written on the CRT, output signals called Z CONTROL are applied to the Z-axis amplifier. One of the Z control signals is ENABLE ZAMP and controls the beam blanking. If the character and/or symbol is to blink, the blink instruction bit is gated with a 2.5 Hz signal. The gated output is a modulated 2.5 Hz ENZAMP signal and is applied to the CRT through the Z-axis amplifier. The Z CONTROL signals also contain intensity information as ZRING and ZNORMAL. These signals, applied to the Z-axis amplifier, provide the drive control voltages for G-1 of the CRT. A manual intensity control provides adjustment for required intensity; however, a photo sensor provides automatic intensity correction for ambient light conditions.

11-61. The display unit CRT deflection circuits, CRT gun control circuits and high voltage are sampled for BIT. If a failure occurs, a DISPLAY FAIL or GUN FAIL signal is produced and a DISPLAY FAIL signal is sent to the computer through the RWR power supply. Also, a SHUTOFF signal from the RWR power supply is applied to the Z-Axis Amplifier through the X and Y D/A Converter. The SHUTOFF signal blanks the CRT if the power supply is shut off as a power off function or as a result of a malfunction.

11-62. **WARNING LIGHTS AND AUDIO CIRCUITS.** See Figure 11-8.

11-63. The caution and launch tones are both enabled during manually started BIT. Launch, a modulated tone, is the only tone audible during manually started BIT unless the TEWS LAUNCH DISABLE switch on the ICCP is pressed and held. Then a caution steady tone is audible. The length of the caution tone depends on the setting of the caution tone timer, while launch tone time length depends on the setting of the launch tone timer. Both the caution and launch tone timers are adjusted at the intermediate maintenance level. On F-15C, when doing a warning lights test of the SAM and Al lights using the LT TEST switch on the INTERIOR LT control panel, the RWR must be on; however, on the F-15D the RWR is not required to be on. Additional data is classified secret. Refer to TO SR1F-15C-2-99GS-00-2, Section 11.

11-64. **BIT CIRCUITS.** See Figure 11-9. The RWR uses four types of BIT to test system integrity. They are Initialization BIT, C-BIT (Continuous BIT), P-BIT (Automatic BIT), I-BIT (Initiated or manual BIT).

11-65. The Initialization BIT is done at power up. The basic system operation is tested and the below specific functions are tested:

a. LRU-2 failure in the CPU, PROM and RAM.

b. LRU-3 failures in the O/P register or the I/P commands.

c. LRU-2, 3 and 6 communications.

d. Scanning hang ups.

e. Constant firing interrupts.

f. Initialization BIT (pass/fail) mode.

11-66. PASS Mode - If Initialization Bit passes all its tests the system continues to scan and process as normal.

11-67. FAIL Mode - If (from power turn-on) it fails any of its tests, the system is not allowed to scan. A branch back to Power-up is done, until Initialization Bit passes. Depending on which test failed it may or may not report the failure. This is discussed in more detail below.

11-68. If (when called from Failure Management Module (FMM)) it fails any of its tests, it will log one of the Initialization Bit fail codes described below and return to FMM and continue to scan.

11-69. Failure of this test will report one or more of the below codes.

Failcode 110 = LRU-2 FAIL
Failcode 111 = LRU-3 FAIL

11-70. Below is a list of the tests that Initialization BIT performs.

1-71. CPU Test - CPU instruction set is tested. A failure of this test will not be logged in Matrix A, Matrix B, Flight Write Prom and will not turn on the NO-GO light. The screen will go blank. The 2nd firing of the Hardware DMT will vector the system back to a cold restart and the process will repeat, as long as the CPU test fails. LRU-2 is set.

11-72. PROM CHECKSUM - Checksum EEPROM is used by Scan Control, Bit, FMM, CSBIT, EXEC, COMSUB/PERMANENT Mapped Area and Initialization Bit. If this test fails no logging of the failure is done, no latches are set, and the RWR NO-GO light on the BIT control panel does not come on because the BIT software is assumed to be suspect. A software branch is taken back to the beginning of Initialization BIT and the process will repeat, as long as the PROM Checksum test fails. This test is not done if Initialization BIT is called from FMM.

11-73. RAM TEST - Verifies Read/Write Ram operation for Ram used by BIT, EXEC, SCAN CONTROL and CALIBRATION. A failure of this test will not log in Matrix A, Matrix B, Flight Write Prom, and will not set latches, or turn on the NO-GO light. A software branch is taken back to the beginning of Initialization Bit and the process will repeat, as long as the RAM Test fails. This test is not done if Initialization Bit is called from FMM.

11-74. The Initialization Bit tests listed below have the ability to log into Matrix A & B, be a confirmed failure, be written into Flight Write Prom, set a fail latch, and turn on the RWR NO-GO light.

11-75. LRU-2 REBOUND - There are two parts to this test.

a. DMA Rebound (Attempts to rebound arbitrary data from the output Channel to each input Channel. Besides testing that the correct words are rebounded, the routine also tests that the correct number of DMA-OUT and DMA-IN complete interrupts are produced.

b. P-BUS Rebound Test - This Rebound does both an upper word rebound and a lower word rebound.

11-76. LRU-2 CONSTANT FIRING INTERRUPT TEST - This routine is called from within the LRU-2 Rebound test and is only done when the LRU-2 Rebound test is called from Initialization BIT.

11-77. This function verifies no LRU-2 Interrupts are firing continuously. To isolate the LRU-2 interrupts, and prevent the LRU-3 interrupts from firing the LRU-2, it is put into the Rebound Mode.

11-78. The LRU-2 interrupts tested are: Memory Parity, End of Window, DMA-OUT, DMA-IN.

11-79. LRU-3 CONSTANT FIRING INTERRUPTS - This routine verifies that no LRU-3 interrupts tested are firing continuously. The interrupts tested are 1ms, SPARE, 41ms, DMT, GSP Overload, ICS, ETASK, RADAR Turnaround.

11-80. LRU-3 ROC/RIC TEST - This test verifies the basic operations/communications of various command address words (CAW's) and their communications lines.

11-81. The below listed CAWS are tested:

CAW16 Receiver Control

CAW18 LRU-6 Data Words

CAW22 C/D Present

CAW24 ETASK

CAW30 High Band Mux Output

CAW34 ICS/CMD Reply

CAW12 Read Screen Processor Status

CAW0D Set Up Mux

CAW03 Initiate Rapid ICS Mode

CAW04 Disable Rapid ICS Mode

CAW23 Read Flag Word

CAW25 Read Data into Processor

11-82. TIME COUNTER VALIDATION - Verify the correct operation of the system time counter. Successive reads of the time counter with a known fixed time delay in between the reads are done. The two times are compared for a positive change in time with tolerance. Both the MSW and LSW words of the time counter are tested.

11-83. LRU-6 REBOUND - Rebounds data from the LRU-2 to the LRU-3/6 INTERFACE.

11-84. This test consists of two parts: A rebound command test and a rebound data test.

11-85. When in the Rebound Command, H/W should always rebound 9855. When in rebound data, whatever data is sent out should be rebounded. Pattern 5555 is arbitrarily used for data.

LEGEND

1. SEE RWR INTERFACE SIMPLIFIED SCHEMATIC
2. ENCODED DATA TRANSMITTED TO THE TEWS DISPLAY UNIT VIA THE DISPLAY DATA WORD. EACH DISPLAY DATA WORD CONTAINS THE FOLLOWING COMMANDS: SYMBOL-POSITION-INTENSITY-CIRCLE
3. SEE RWR BIT CIRCUITS SIMPLIFIED SCHEMATIC
4. SEE RWR POWER DISTRIBUTION SIMPLIFIED SCHEMATIC

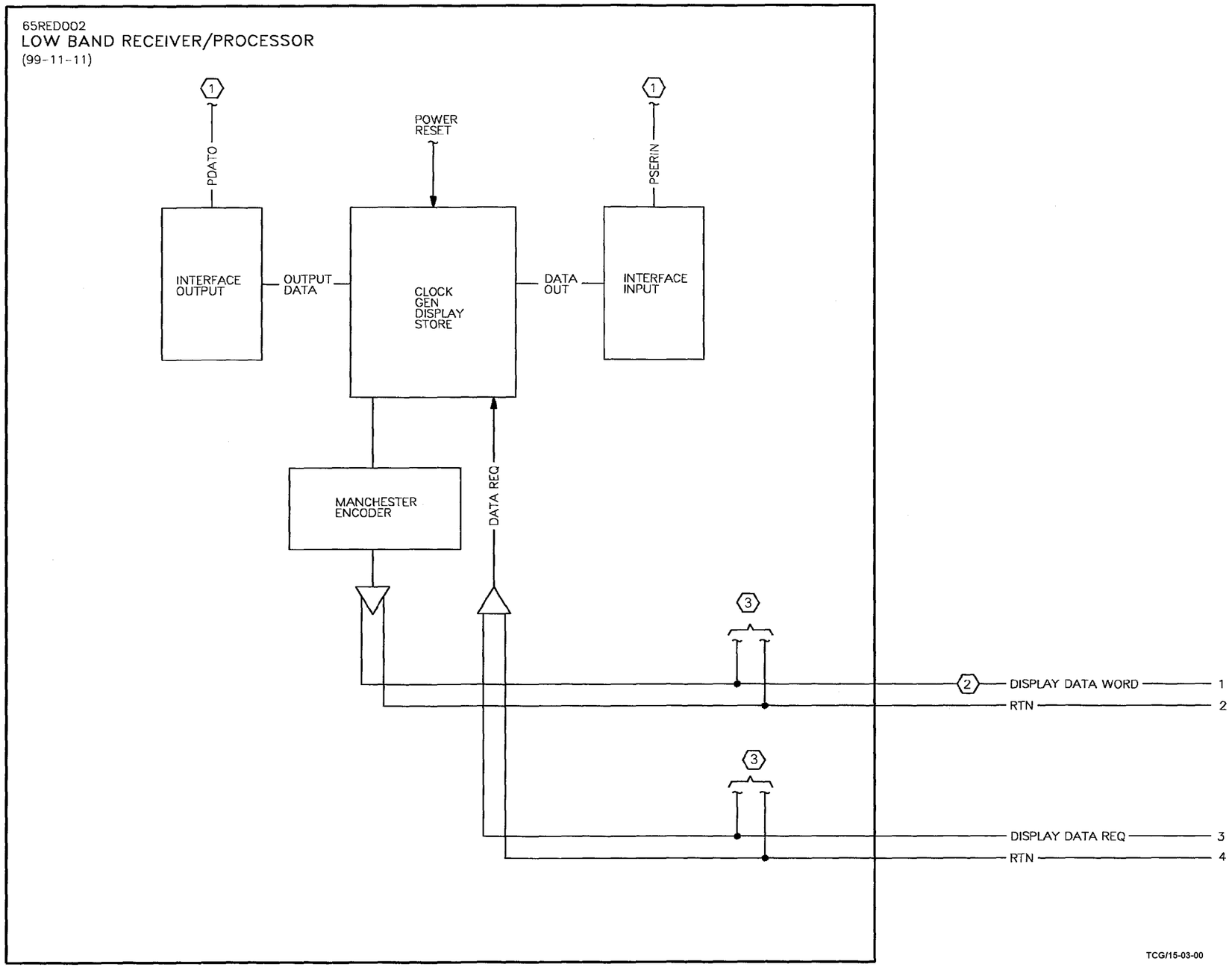


Figure 11-7. RWR Display Circuits Simplified Schematic (Sheet 1 of 3)

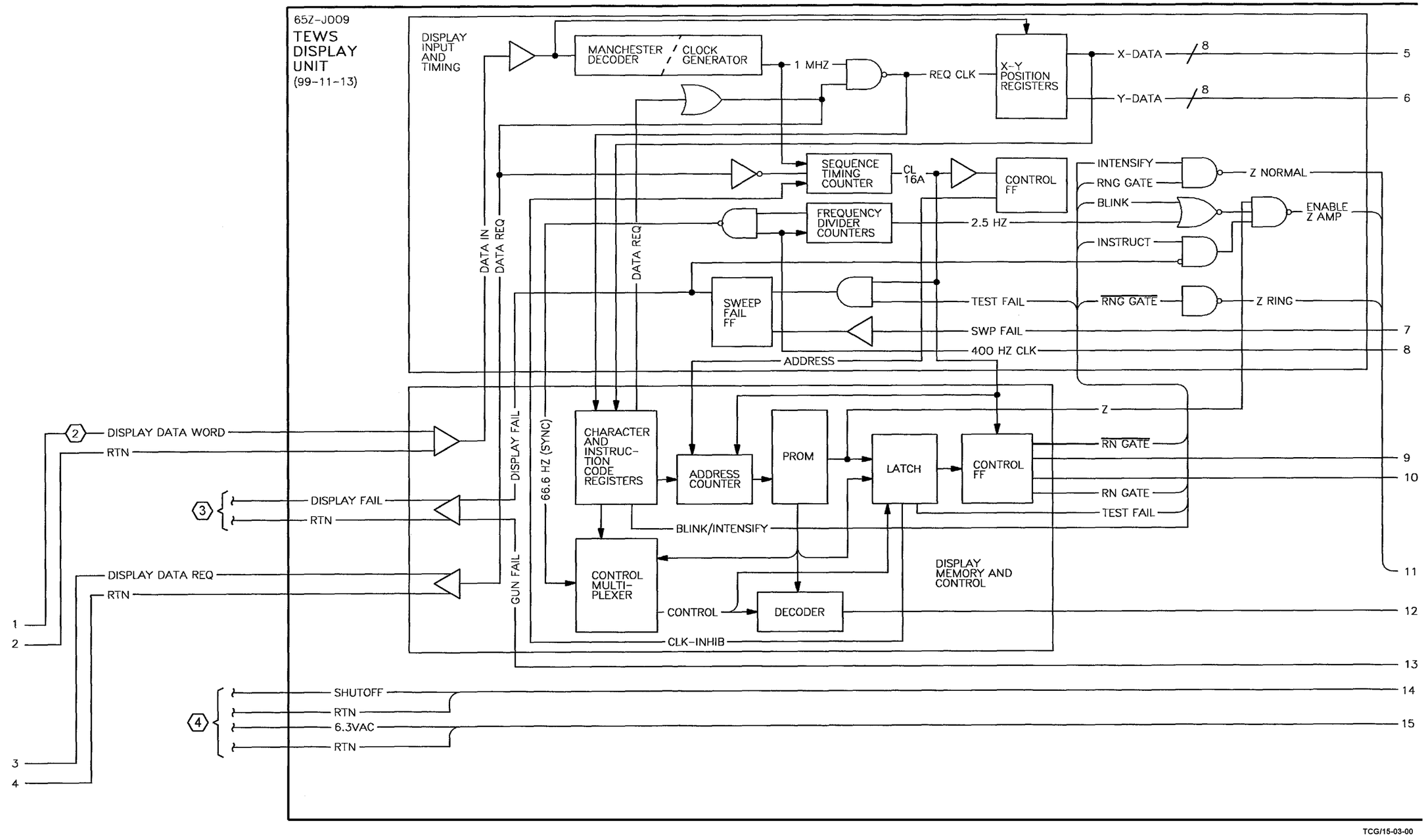


Figure 11-7. RWR Display Circuits Simplified Schematic (Sheet 2)

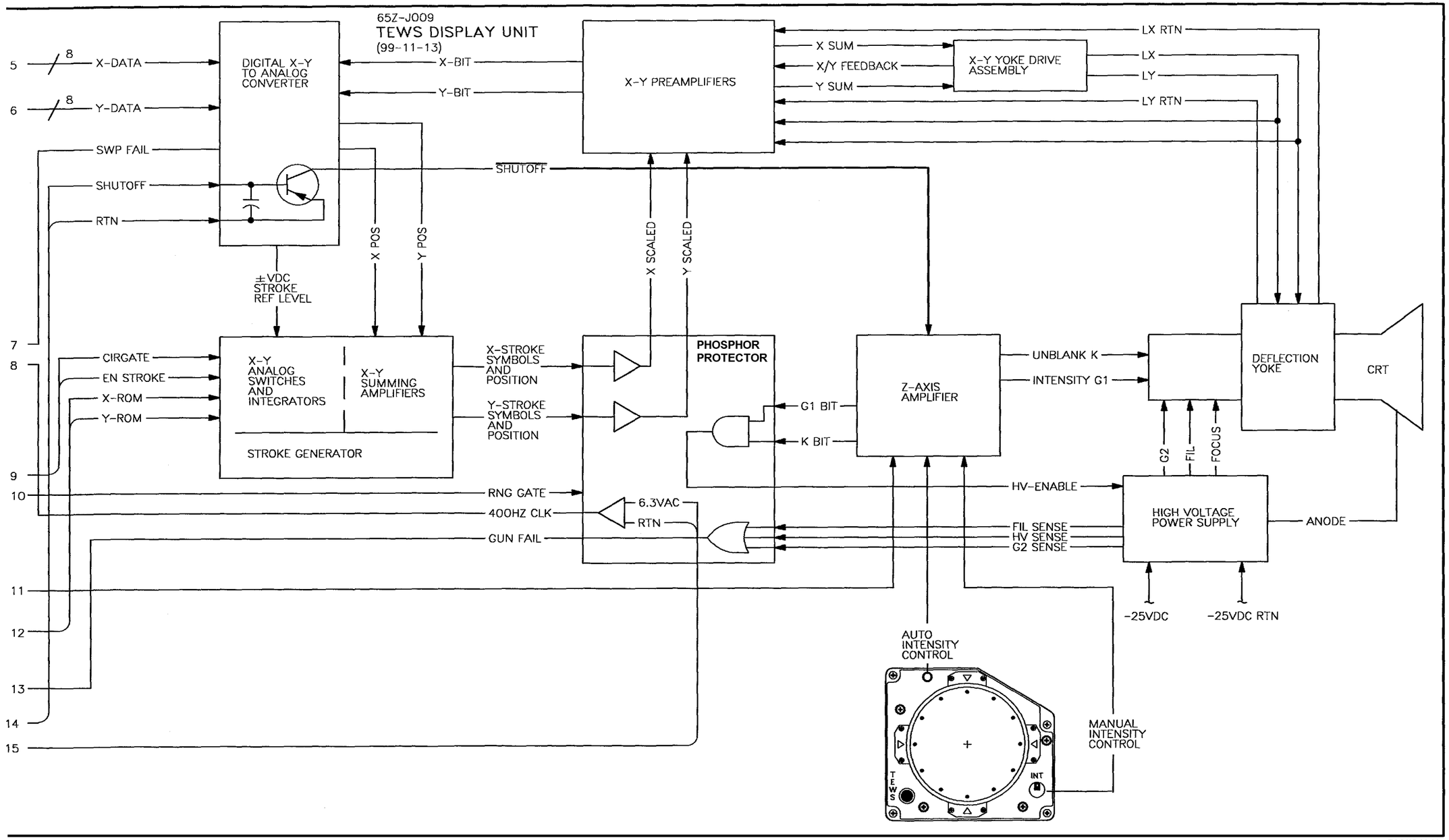


Figure 11-7. RWR Display Circuits Simplified Schematic (Sheet 3)

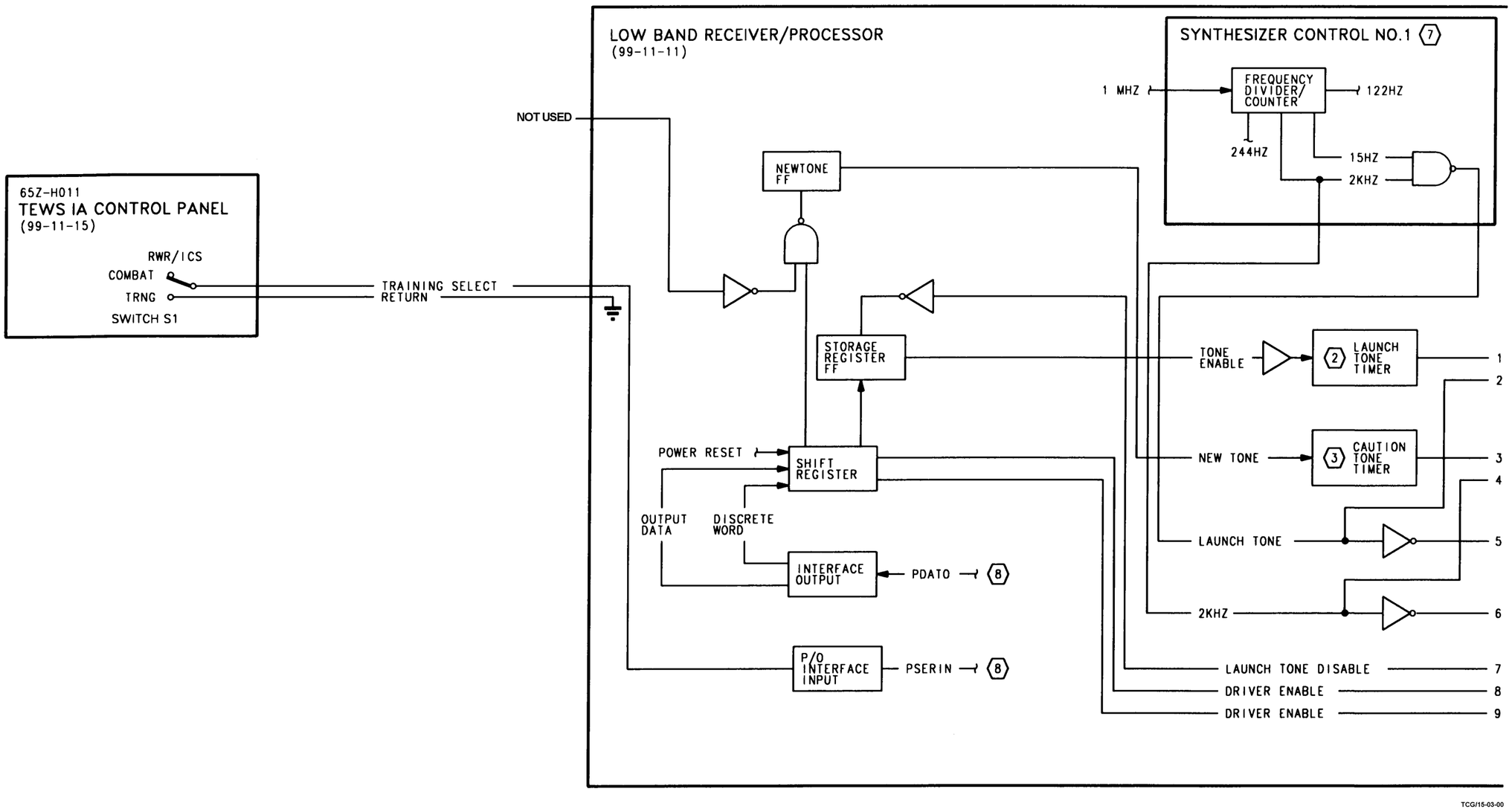


Figure 11-8. RWR Warning Lights and Audio Circuits Simplified Schematic (Sheet 1 of 3)

65RED002
LOW BAND RECEIVER/PROCESSOR
(99-11-11)

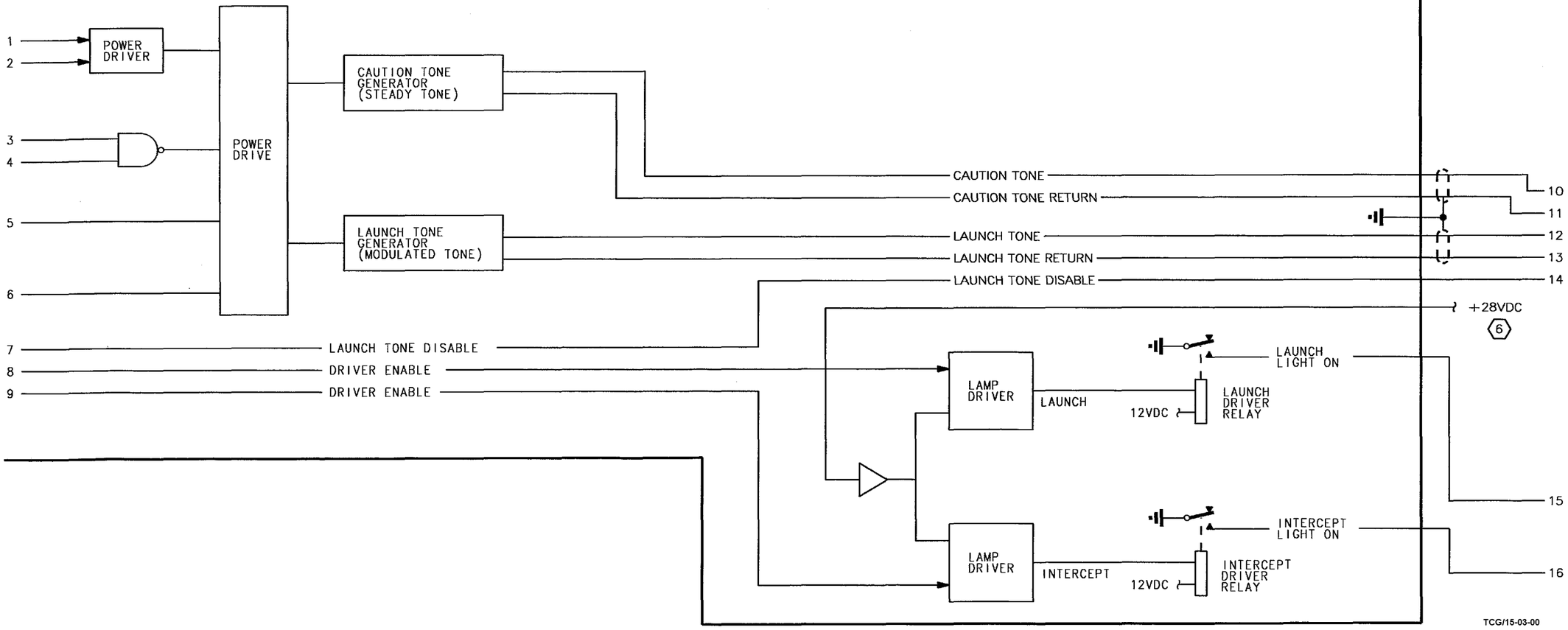


Figure 11-8. RWR Warning Lights and Audio Circuits Simplified Schematic (Sheet 2)

LEGEND

(1) RELAY ENERGIZED BY LIGHTS TEST SWITCH OPERATION.
(2) LAUNCH TONE TIMER (MAINTENANCE ADJUSTABLE FOR CONTINUOUS MODE OR 2-15 SECONDS).
(3) CAUTION TONE TIMER (MAINTENANCE ADJUSTABLE 2-10 SECONDS).
[4] F-15C.
[5] F-15D.
(6) +28VDC ENERGIZED BY LIGHTS TEST SWITCH OPERATION.
(7) SEE RWR BIT SIMPLIFIED SCHEMATIC.
(8) SEE RWR INTERFACE SIMPLIFIED SCHEMATIC.

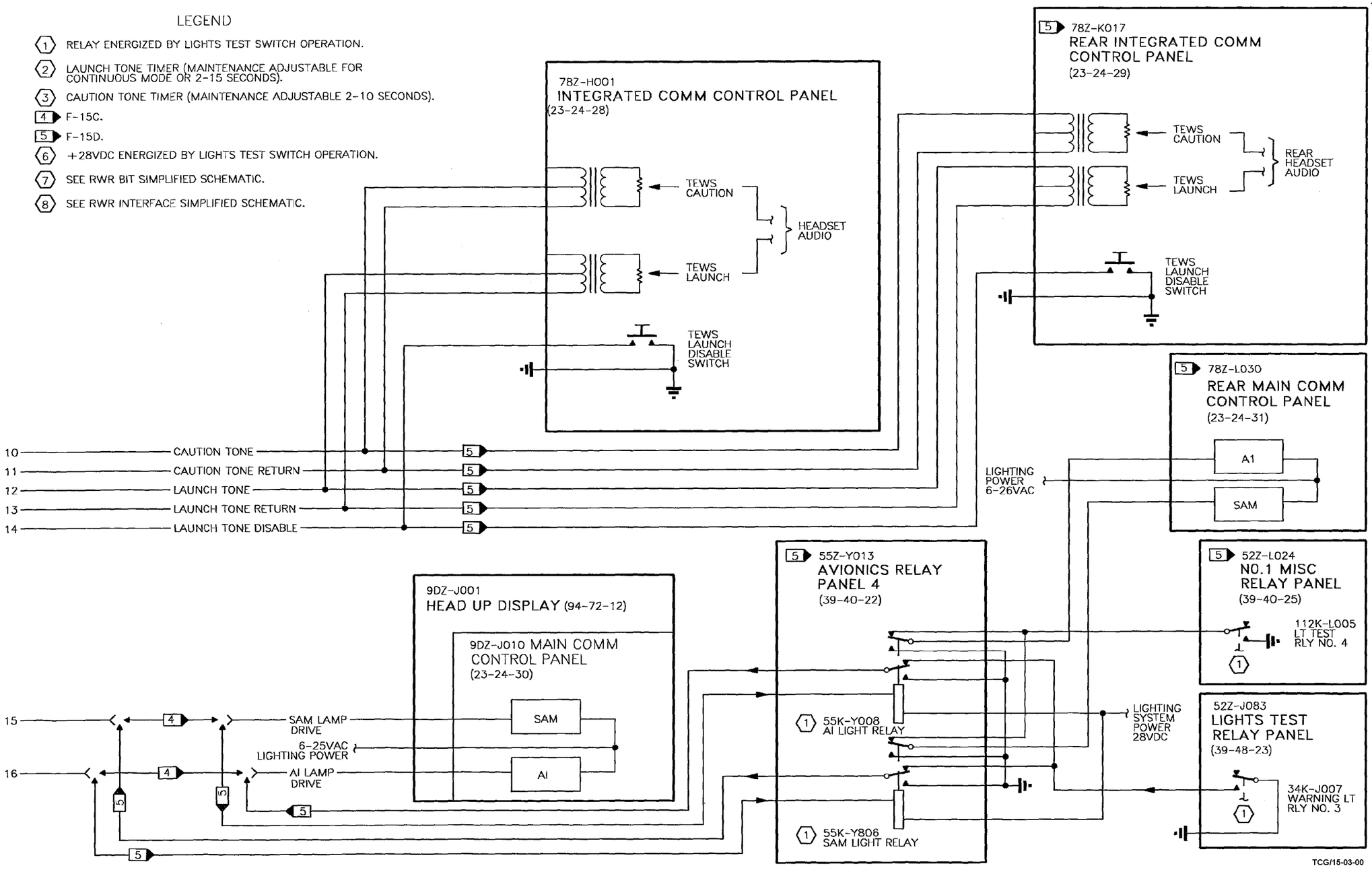


Figure 11-8. RWR Warning Lights and Audio Circuits Simplified Schematic (Sheet 3)

11-86. Continuous BIT. Continuous BIT monitors the voltages and tests for short circuits throughout the RWR. If a short exists the power supply will shut down the LRU associated with the short. Continuous BIT is done at the end of each scan.

11-87. Automatic BIT. Automatic BIT monitors the operation of an AN/ALR-56C RWR system by doing periodic tests of RWR functions. BIT verifies that an end-to-end RWR function is working, rather than to test individual LRUs or hardware components. Additional diagnostic tests to fault isolate failures to a particular LRU are done only when an end-to-end function is not working.

11-88. The BIT tests are all software controlled. The BIT is a task invoked by the operational flight program (OFP). Existing implementation divides the BIT tests into three segments, with a segment of tests being approximately every 4 seconds. Thus, the complete battery of BIT tests (referred to as a BIT cycle) are approximately every 12 seconds. A BIT segment is invoked only when the OFP scan has reached an end of break, when the receiver and Direct Memory Access (DMA) lines are not being used by any other OFP function except possibly to receive SI (Scan Illuminator) data. A BIT segment will not be done if BIT is called during a scan restart sequence.

11-89. When a BIT test detects a failure, a failure report is issued and any diagnostic testing that is required for fault isolation is done. Because ambient and temporary conditions may cause a test to fail when the system is actually fully functional, BIT will not immediately set a fail latch or report a system failure. Rather, BIT applies the Double “5 of 7” rule. This requires an LRU to display a failure during two consecutive five out of seven BIT failure cycles (approximately 3 minutes of operation) before a system failure will be declared or a latch will be set. No latches are set during the first 5 minutes after power on to allow for normal system warm-up. At the end of the 5-minute warm-up, all fail counters are reset, therefore it will take approximately an additional 3 minutes before a latch is set.

11-90. After an LRU has been declared faulty, BIT will continue evaluating system performance to monitor either further deterioration or recovery. Recovery of a failed LRU is defined as not displaying a failure for three consecutive BIT cycles. If no failures are discovered for three consecutive BIT cycles, the pilot’s RWR fail light will be turned off. Any LRU latches that were set will, of course, remain set which indicates that a failure did occur.

11-91. BIT maintains two buffers where failure reports are stored. The first buffer, BIT matrix A, contains reports for all failures detected in the BIT cycle. When End of Cycle processing declares a failure or an abort processing condition it is re-initialized by resetting its write pointer to its first word and by clearing out the buffer.

11-92. The second buffer, BIT Matrix B, contains reports for confirmed failures; i.e., those failures that have met the Double 5/7 rule and therefore caused a latch to set. It also contains reports for failures that met the first 5/7 rule but not the second and therefore did not get confirmed. To implement this, after a BIT cycle in which an LRU has been determined to be faulty by the 5 of 7 rule, all failure reports in matrix A that are attributed to the failed LRU are appended onto matrix B.

11-93. BIT Matrix B is a circular buffer. Both buffers can contain up to 20 failure reports.

11-94. During the course of a mission, the contents of BIT Matrix B are copied into Flight Write EEPROM at the rate of one word every 4 seconds. The contents of flight write can be determined either by examining flight write memory directly by displaying its contents on LRU-9 (for F15-C aircraft). Details on how to display flight write information is contained in TO SR1F-15C-2-99JG-11-1 (99-11-05 and 99-11-06).

11-95. There are some failure reports that appear in the BIT matrices that will not cause latch settings and were not produced by a BIT function test. These asynchronous failure reports are produced elsewhere in the OFP when certain failure conditions are noted. An asynchronous failure report is processed through BIT Matrix A and B.

11-96. Within the OFP, eight modules are dedicated to BIT functions. The module BIT contains the BIT test scheduler and the BIT periodic tests. The module Failure Management Module (FMM) does failure isolation, accounting of the frequency of failures, posting in BIT matrices A and B, as well as lighting the RWR fail light on the BIT control panel and setting latches on the associated LRU. The module CSBIT contains subroutines for BIT and FMM. COMBIT contains the computer BIT test. CXEEPR executes the Checksum test, and MVERAM does the RAM test

Initialization Bit tests out basic LRU-2 and LRU-3 functions including interface between the LRU-2, LRU-3, and LRU-6. Finally, BITWRT is called to copy the contents of BIT Matrix B to EEPROM. Some BIT subroutines are located elsewhere in common OFP areas as well.

11-97. DOUBLE 5/7 failures. Matrix A Failure Buffer for the failcode or fail codes related to the same failed LRU that have met the 1st 5/7 failure criteria are passed to Matrix B. On the second successive 5/7 BIT failure cycle of the same fail code or fail codes, the RWR NO-GO light on the BIT control panel comes on, the failure latch on the LRU is set and a failure is written to Flight Write PROM.

11-98. During the 5 minute warm-up (on power turn-on) BIT is running as normal. Failures if any will log in to Matrix A. This means that failures are not passed to Matrix B or to Flight Write PROM. The RWR NO-GO light on the BIT control panel does not come on and LRU latches will not set. At the end of each cycle Matrix A is cleared and BIT starts a new cycle. At the 5 minute point all failures logged in Matrix A are cleared, LRU histograms are cleared and BIT will now log failures for real.

11-99. FLIGHT WRITE PROM/LATCH SET. Entries are written to Flight Write PROM on the 2nd consecutive confirmed 5/7 Failure Cycle (of the same fail code/s) and at the same time the applicable latch is set. If the 2nd consecutive confirmed 5/7 Bit Failure Cycle does not occur the entry will not be put into Flight Write PROM and the latch will not be set.

11-100. RWR LIGHT. On the 2nd consecutive confirmed 5/7 Bit Failure Cycle the RWR light on the BIT control panel is turned on. With no BIT detection test failures detected for a minimum of three consecutive Bit cycles the system is declared good, and the RWR light is turned off.

11-101. BIT DWELLS. Many BIT tests involve tuning the receiver, opening a dwell and examining the pulses received in video data. Unless otherwise noted in a specific test description, the below information regarding any BIT dwell is true.

11-102. No parameter set words are included in the tuning words. Two screens are included. The first is an accept screen with wide-open RF and pulsewidth limits, and DF limits set to accept only antenna 1 of 2, depending on which channel is being used. The second screen is a wide-open reject screen that will reject anything not accepted by the accept screen; this will make sure that no garbage group statements are produced. Both screens have the pulse buffer reject function enabled.

11-103. Histograms are cleared after every dwell. The receiver is tuned to a standard frequency, which is the one used in the first Frequency Coverage Test dwell. The signal source is usually the fixed picket (comb generator), and dwells are generally done in medium-bandwidth mode. Most dwells are not auto-increment. Dwell time allows four pulses to be received.

11-104. The video filter switch is off. The IF preamplifier is off. The amplitude and frequency rate histograms in the video processor are off. The video processor is set to stare at the desired antenna. The RF bypass is disabled. The SPU bypass is enabled. Video processor pulse-width limits are set to accept only the maximum pulse width. In order to receive pulse data from the CW signal source, leading edge bypass is enabled. RF coincidence is set to reject. Medium-bandwidth discriminator correction values are included in the tuning words for all medium and narrow-bandwidth dwells.

11-105. Before troubleshooting any hardware failure using BIT, two areas must be fully understood. The first area is the overall structure of BIT, including its frequency of execution, definitions of periodic tests, asynchronous failure reports, diagnostic tests, and general procedures for resolving fault isolation ambiguities. The description of BIT contained earlier in this overview provides sufficient information regarding this area.

11-106. The second area concerns the BIT failure report Matrices A and B. This includes the algorithms for posting failure reports in the matrices and the structure of a failure report. The codes employed in the failure reporting are described in TO SR1F-15C-2-99JG-11-1 (99-11-06).

11-107. With this information, one can monitor BIT's evaluation of system performance, knowing which BIT tests have failed and to which LRUs the failures are being attributed. This information can be better understood by being familiar with the method of the failed test. The tuning words provide further details on the configuration of the system during these tests.

11-108. The final step is to use the BIT results to locate the precise hardware failure. This can often be a

painstaking process. This manual provides two features to assist in this phase. The first is the inclusion of a Most Likely Failures list with each test description that identifies the most likely candidates for hardware failure in case of failure of the associated test. Note, however, that these lists are only the most probable failures; the lists are by no means complete or definitive, since any variety of hardware failures can often affect BIT in unforseeable ways. The Most Likely Failure lists, therefore, should be used only as a guide. It should be noted that in addition to the information revealed by BIT, insight into the state of a system can also be obtained by monitoring the performance of the OFP calibration functions.

11-109. ANTENNA TEST. Checks for presence of the four high-band and one low-band antennas. For each high-band antenna, the high-band antenna BIT mux is used to test for a DC load on the antenna port. The same is done for the low-band antenna using the data link mux. If all antennas are present, the test passes; if any antenna is not present, a failure report is issued.

11-110. The high-band antenna BIT is not done if communication with LRU-6 is not possible.

11-111. Failure of this test will report one or more of the below codes.

59 LRU-5L (antenna 1) failure; no diagnostic.

60 LRU-5R (antenna 2) failure; no diagnostic.

61 LRU-7R (antenna 3) failure; no diagnostic.

62 LRU-7L (antenna 4) failure; no diagnostic.

63 LRU-8 (low-band antenna) failure; no diagnostic.

11-112. BANDWIDTH AMPLITUDE TEST. This test will verify the equivalence of amplitude reports for wide and medium-bandwidth reports. The variable picket is first turned to the standard frequency in Channel A. If the picket cannot be tuned, this test is not done. The average amplitude seen when the reciever was tuned in wide bandwidth (during the tune-variable-picket process) is recorded. Using the same Channel A attenuation setting and the same variable picket tuning value, a dwell is then enabled in medium-bandwidth mode. If no signal is seen, a failure report is issued. The average amplitude seen in the medium-bandwidth dwell is then compared to that of the wide-bandwidth dwell. If the two amplitudes are too far apart, a failure report is issued.

11-113. This test is only done if the Frequency Coverage Test at the standard frequency in Channel A passed. This test will report one or more of the below fault codes.

106 No signal in medium-bandwidth dwell.

107 Wide and medium-bandwidth amplitudes too far apart.

11-114. CHANNEL ONE TEST This test will verify the proper functioning of DMA Channel One. Whenever the scan regime enables DMA Channel One, it sets a flag indicating whether or not the channel became active. This test first tests the status of this flag; if it indicates that the channel did not become active when it should have, a failure report is issued and the remainder of the test is omitted.

11-115. The remainder of the test is not done if Channel One is not active or if the Frequency Coverage Test in Channel A at the standard frequency failed. A Channel A dwell at the standard frequency is enabled, directing the video data to come in as SI data via DMA Channel One and using the fixed picket as the signal source. (Pulses from this dwell are recognizable among other SI pulses by their unique pulse widths and screen IDs). Dwell time allows for six pulses. If less than four are received, a failure report is issued, and the LRU-2 Rebound Test is done as a diagnostic.

11-116. Failure of this test will report one or more of the below codes.

102 No signal seen.

103 Channel One did not go active.

This test is the only BIT test that uses DMA Channel one. All other channels use Channel Zero for video data and Channel Two for group statement data (if required).

11-117. CMD REBOUND TEST. This test will test the CMD (Countermeasures Dispenser) data link. A test is made to determine if there has been a communication failure between the CMD and the RWR. If there hasn't, the rebound test is not done. If there has, and the Manchester link to the CMD is present, the rebound test is attempted.

11-118. The rebound test rebounds the pattern E000 through the CMD interface via the data link mux. If the pattern word rebounds correctly, the test passes. If not, flags are set indicating no Manchester link and rebound failure, and a failure report is issued indicating the

expected and received pattern words. An LRU-3 fail latch is also set.

11-119. The data link is reset to ICS 1 input at the completion of this test. Failure of this test will report the below code.

67 Incorrect rebound data received for CMD. Since any word sent to the CMD interface is outputted to the CMD as well, the pattern word for this test was deliberately set to a value that would not be misinterpreted as a data word by the CMD.

11-120. COARSE CW TEST. This test will test ability of CW path to pass a signal and report correct RF tags. A three-step, coarse CW, auto-increment dwell is done, using the fixed picket as the source signal at the standard frequency, and routing the signal through the CW path in LRU-3. The CW dwell should allow eight pulses through.

11-121. Video data for the dwell is expected to show that at least six of these pulses were seen, and that the signal was only seen in the middle step of the dwell. If no signal is seen, or if the signal was seen in either of the other steps, a failure report is created.

11-122. If the signal was seen in the wrong step, the failure report will include the bad RF tag.

11-123. The test is done in both channels A and B. Note that in coarse CW, the video processor must have both channels enabled whether operating in Channel A or in Channel B.

11-124. A no-signal failure report is sent to the failure management module only if the Frequency Coverage Test at the standard frequency for the failed channel passed (indicating that the signal path out of LRU-6 is intact) and if VCO calibration passed. A bad RF tag failure report is sent only if VCO calibration passed.

11-125. To prevent spurious noise from leaking into the dwell and generating pulses with improper RF tags, the Coarse CW Test is done using as high attenuation as possible. During the first Coarse CW Test execution, attenuation is initially set to its maximum level and then successively dropped five counts at a time until the signal is seen; a tolerance of another 20 counts is then subtracted to obtain the optimal attenuation value to use in this and subsequent executions of this test. The attenuation values obtained here are also used by other tests that use the fixed picket as their signal source and are sensitive to slight variations in RF. These other tests include the Fine CW Test and all Screen Processor Histogram Test dwells. Whenever the Coarse CW Test or any of the other tests fail, the attenuation value to use for the channel that had the failure is recalculated during the next Coarse CW Test execution.

11-126. Failure of this test will report one or more of the below codes.

17 No signal in Channel A.

18 No signal in Channel B.

19 Improper RF tag seen.

11-127. COMPUTER BIT TEST. This test will verify the proper functioning of the CPU. The computer BIT is activated by outputting a CAW 3A. This stimulates an interrupt No. 11 whose interrupt handler invokes the computer BIT code. The Computer BIT code does the below groups of tests on the CPU. All registers are tested to see that they can be written into and read from. All addressing modes are tested. The operation of the condition code register and overflow flag is tested. All LPP-128 instructions are tested for proper operation.

11-128. If a test passes, computer BIT will sequentially continue with the next test. If a test fails, however, the code will hang in an infinite loop.

11-129. The initiation of computer BIT activates a timer that will set the LRU-2 latch after about 8 ms, unless a CAW 3F is issued first. The last instruction in computer BIT is the output of a CAW 3F. If all tests pass, this CAW 3F will be reached with the 8-ms limit, and the LRU-2 latch will not be set. If the code falls into an infinite loop because of a test failure, however, the LRU-2 latch will be set after 8 ms are up. The code will then remain in the infinite loop until the system dead-man timer (DMT) fires.

11-130. When the DMT fires, the DMT interrupt handler will issue a failure report that includes the address of the infinite loop. (The infinite loop is located shortly after the failed test.) A flag enables the failure management module to distinguish between regular DMT firings and those caused by computer BIT.

11-131. This test will report the below failure code. 13 Computer BIT Test failure. In addition to the scheduled computer BIT execution once per BIT cycle, computer BIT will be done every time a memory parity interrupt occurs.

11-132. CRITICAL FLAGS TEST. This test will test the status of critical flags that indicate current state of system. Three flags are tested as part of this test.

a. Group Statement Received Flag - indicates whether the Group Statement Processor is writing group statements into the group statement buffer. If it isn't, the LRU-2 Rebound Test is done to fault isolate between LRU-2 and LRU-3, and a failure report is issued.

b. Pulse Buffer Reject Flag - indicates whether the Group Statement Processor is generating group statements for dwells that have the pulse buffer reject function enabled. If it is, a failure report is issued. The first dwell of the Screen Processor Parameter Limits Test is done with a parameter set (using the dwell ID 0) and pulse buffer reject enabled. Group statements being produced by this dwell will be indicated by this flag.

c. CC Communications Flag - indicates whether the RWR is receiving data from the on-board central computer. If it's not and the Manchester link to the CC is present, then a test is made of how many times this failure has been noted. If the number of occurrences is greater than ten, the LRU-2 Rebound Test is done to fault isolate between the LRU-2 and LRU-3, and a failure report is issued.

11-133. Failure of this test will report one or more of the below codes.

6 Group Statements not received.

7 Pulse Buffer Reject function not operating.

71 No communication with the CC.

11-134. DISCRIMINATOR CALIBRATION TEST. This test will test if the Discriminator Calibration passed and attempt to recover in case of failure. Nothing is done if the last execution of Discriminator Calibration passed. The calibration is reattempted if it failed the last time. Again, nothing is done if it passes on the second attempt. Otherwise, a failure report is issued.

11-135. The failure reports for failing all steps and for no signal from the variable picket are only issued if the Channel B Frequency Coverage Test at the standard frequency passed (indicating the intactness of that signal path in medium band). No failure report is issued if the previous gain, VCO, or limiter calibrations failed.

11-136. Failure of this test will report one or more of the below codes.

75 Discriminator calibration received no signal in any step, although the variable picket's signal was seen.

76 Variable picket could not be tuned (did not see signal).

77 Discriminator calibration received no signal in some steps.

78 Tag seen very far from expected value.

92 No edge of wideband found.

For codes 77 and 78, the failure report diagnostic data includes only the first RF tag to fail. Further investigation is required to determine the full extent of the calibration failure.

11-137. DOUBLET ACCEPT AND REJECT TEST. This test will test the systems ability to accept and reject doublets based on PPI value. Two dwells are done, both using the BIT oscillator in LRU-3 as the source signal, routing it into the wideband IF path in Channel B. The video processor chops the source signal to a size that is less than the value associated with the doublet PPI mode 3; hence, this signal source in this mode simulates the presence of a doublet signal.

11-138. In the first dwell, the doublet accept mode 3 is selected, which should allow exactly one pulse to be accepted. Current test tolerance allows three pulses. If more are seen, a failure report is issued. If no signal is seen, a failure report is issued, and the LRU-2 Rebound Test is done as a diagnostic.

11-139. In the second dwell, the doublet reject mode 3 is selected, which should reject all pulses with PPIs below the associated value. Therefore, no data should be received for this dwell. If any pulses are seen, a failure report is issued. This test is not done if the Threshold Test did not see a signal. Also, in present implementation, the second dwell is not done if the first failed. This test will report one or more of the below failures.

52 No signal in accept dwell.

53 Too many pulses received in accept dwell.

54 Pulses received in reject dwell.

11-140. EEPROM CHECKSUM TEST. This test verifies the authenticity of software loaded. For an LPP-256 computer, 180K of system EEPROM are

divided into 22 blocks of approximately 8K each. One such block is tested in each BIT segment; therefore, since a BIT segment is executed every 4 seconds, all of EEPROM is tested every 88 seconds.

11-141. For each block under test, the EEPROM test applies a checksum function to its contents; obtaining a 16-bit word as the result. The checksum obtained during test is compared to the stored, expected checksum for that block.

11-142. Not computing the expected checksum for any block constitutes an EEPROM test failure. Should this occur, a failure report is produced containing a code that indicates the failed memory block, the calculated checksum, and the expected checksum.

11-143. On successful completion of the test for a block, counters are set to continue with the next block during the next BIT segment. On a failure, the counters are set to retest the failed block during the next segment.

11-144. The checksum function used is the below: temporary checksum value is initially set to the address of the first location in the memory block. For each location in the memory block, the temporary checksum value is modified by successively exclusive-or'ing it with the location's contents and shift-right-rotating it once. The value of the temporary checksum at the end of a block is then the checksum for that block.

11-145. To limit the execution time of a BIT segment, the EEPROM test is not immediately done during a segment. Rather, it is scheduled to be executed 2 seconds later. This assures that it will be completed before the start of the next BIT segment, but that it will be run at a time when the OFP can afford the computer time. Since this test does not do a dwell, it will not interfere with the portion of the scan that will be active then. A flag is used to prevent rescheduling the test if the previously scheduled test hasn't been done yet.

11-146. This test will report the below listed failure codes. 4 Calculated checksum not equal to stored checksum. The first diagnostic data word in an EEPROM test failure report is a code indicating the failed memory block. Interpretation of the code is given by the table below.

11-147. For LPP-256 computers

Code	Memory Area
0	IAM OFP (from location contained in 4000 to location contained in 4001)
1	IAM PFM (from location contained in 4003 to location contained in 4004)
2	First location after flight (currently 9065) to 9FFF
3	A000 - BFFF
5	C000 - DFFF
6	E000 - FFFF
7	10000 - 11FFFF
8	12000 - 13FFF
A	14000 - 15FFF
B	16000 - 17FFF
	18000 - 19FFF
D	lA000 - 1BFFF
F	1C000 - 1DFFF
10	lE000 - 1FFFF
	20000 - 21FFF
	22000 - 23FFF
	24000 - 25FFF
	26000 - 27FFF
16	RWR Scan PFM (from location contained in 28000 to location contained in 280001)
17	RWR Threat PFM (from location contained in 2A000 to location contained in 2A001)
18	RWR Dwell ID Tables (from location contained in 2C000 to location contained in 2C001)
19	2C800 - 2DFFF
1A	2E000 - 2FFFF

11-148. The addresses specified under memory area locations above are page addresses.

11-149. FINE CW TEST. This test will test the system's ability to pick up a Fine CW signal and accurately report its RF tag. An auto-increment dwell is done in Channel A in very narrow bandwidth that uses the Fine CW filter, taking its source signal from the fixed picket. Eight pulses are expected; if less than six pulses are seen, a failure report is issued. If six or more pulses are seen, then the RF tags of the pulses are tested. If any of the tags are outside of the acceptable range or if too many different tags were seen, a failure report is issued indicating the bad tags or the number of tags, respectively. The test is not done at all if VCO calibration failed.

11-150. No signal failure report is only reported if the Coarse CW test passed (which indicates that the signal path outside the Fine CW filter is intact).

11-151. The VCO tuning values for this dwell are every LSB covering the width of a narrow bandwidth.

11-152. The attenuation setting for this dwell is the value determined during the Coarse CW test to be appropriate for tests that use the fixed picket and are RF sensitive. Threshold is determined as function of the amplitude seen during the Coarse CW tests to ensure seeing only the center signal. Since a Fine CW signal does not pass through the channelizer and it is not desired that a spurious signal in the channelizer cause the Fine CW signal to be rejected, the dwell is done with RF coincidence set to accept.

11-153. Failure of this test will report one or more of the below codes.

20 No FCW signal.

Dwell	LO
1	None
2	1
3	2
4	3
5	2

21 Received RF tags that are outside expected range.

22 Too many RF tags were seen.

11-154. FREQUENCY COVERAGE TEST. This test will test for proper functioning of all LOs, Mod I filters, Mod II filters, and IF path for both channels. Using the fixed picket as the source signal and operating in medium bandwidth, five dwells at five different frequencies are done in each channel. The five frequencies were selected in a fashion that ensures that every LO, Mod I filter, and Mod II filter is used at least once in this test.

11-155. The sequence in which the components are tested is as follows:

Mod I Filter	Mod II Filter
None	5
1	2
2	3
3	4
4	1

11-156. The dwell time for each dwell allows six pulses to come in. If at least four of these are received in video data, the signal path under test is considered to be intact; receiving fewer pulses constitutes a failure.

11-157. If the dwell at any frequency failed, the remaining frequencies will still be attempted. After the five dwells for a channel have been done, if any frequency had failed, a failure report is created and the IF test for the failed channel is done to fault isolate the failure. The failure report for codes 9 and 10 will include the first three frequencies that failed.

11-158. Failure of this test will report one or more of the below codes.

9 Only some Channel A dwells saw the signal.
10 Only some Channel B dwells saw the signal.
11 No Channel A dwell saw the signal.
12 No Channel B dwell saw the signal.

The first character of the failure code word in the failure buffer will indicate which LRU it considers at fault. That, along with knowledge of which channel had the failure, knowledge of which dwells failed, plus the above chart, together point rather specifically to the failed component. Note that because of hardware design, a failure in the switch-amplifier-switch in LRU-3 will be diagnosed as an LRU-6 failure.

11-159. GAIN CALIBRATION TEST. This test will test IF Gain Calibration passed and attempt to recover in case of failure. If the last execution of Gain Calibration passed, nothing is done. If it failed, the calibration is redone. If it then fails a second time, a failure report is issued.

11-160. Failure reports for low-band failures are only

issued if the Low-Band Test passed (indicating intactness of the low-band signal path).

11-161. A failure report for high-band failure to see a signal is only issued if no signal was received anywhere in the calibration and some of the Frequency Coverage Test steps passed (indicating that the failure is not in the signal path).

11-162. Failure reports for high-band failure to obtain correct attenuation is only issued if some of the Frequency Coverage Test steps for the failed channel passed (indicating that the failure is not in the signal source path).

11-163. Failure reports for too high system noise are issued regardless of the results of other tests. Current BIT implementation assumes the source of the noise to be in LRU-3, because this most frequently is the case.

11-164. Failure of this test will report one or more of the below codes.

86 Low-band failure to receive signal.
87 Low-band failure to obtain correct attenuation.
88 High-band failure to receive signal.
89 High-band failure to obtain correct attenuation in Channel A.
90 High-band failure to obtain correct attenuation.
91 Unable to eliminate system noise.

11-165. Gain Calibration failure codes note only the first event that causes the calibration to fail. Closer investigation is required to determine the full extent of the calibration failure.

11-166. GROUP STATEMENT TEST. This test tests that the Group Statement Processor (GSP) issues correct RF, DF, and pulse-width reports. The fourth dwell of the Screen Processor Histogram Test is done with a parameter set (using dwell ID FF) and should cause six group statements with different RF's to be produced GSP software in the OFP recognizes these group statements and, rather than processing them normally, extracts the RF, DF, and PW data from each and stores it in a special buffer. Because the Screen Processor Historgram test is done in the second BIT segment and the Group Statement Test is done in the

first BIT segment, the buffer should be filled anew before every execution of the Group Statement Test.

11-167. The Group Statement Test tests that RF, DF and PW data stored in the special buffer is consistent with what is expected from the fourth Screen Processor Histogram Test dwell. If any of the data varies by more than a tolerable amount, a failure report is issued. The diagnostic data of the failure report will indicate the original numbers of the failed group statements.

11-168. This test is done if the last execution of the fourth dwell of the Screen Processor Histogram Test failed since proper group statements would then not have been produced.

11-169. Failure of this test will report the below code.

8 Incorrect group statement data.

11-170. ICS REBOUND TEST. This test tests the ICS data link. For each ICS set, a test is made whether there has been a communication failure from that set to the RWR. If there hasn't, the rebound test is not done for that set. The test is also done if the set is in band 1 or 2 and is executing its own intermittent BIT test. Otherwise, the rebound test is done.

11-171. The rebound test rebounds the pattern 1FFE through the ICS interface board via the data link mux. If the patter word rebounds correctly, the test passes. If it doesn't, flags are set indicating no Manchester link and rebound failure, and a failure report is issued indicating the expected and received pattern words. A fail latch for the LRU-3 is also set.

11-172. The test is done in both rapid and normal ICS modes with a specified delay between modes.

11-173. The data link is reset to ICS1 input at the completion of this test.

11-174. Failure of this test will report one or more of the below codes.

64 Incorrect rebound data received for ICS set 1.
65 Incorrect rebound data received for ICS set 2.
65 Incorrect rebound data received for ICS set 3.

The rebound word used has incorrect parity and will be rejected by the ICS.

11-175. JAMMER DELAY CALIBRATION TEST. This test tests if the Jammer Delay Calibration passed. If the last execution of Jammer Delay Calibration passed, nothing is done; otherwise, a failure report is issued.

11-176. Since this calibration can fail due to malfunctions of either the RWR or the ICS, and there is no means to distinguish between them, the BIT software decleares this failure unattributable, This will cause the failure to be posted in the failure buffers but

will not set the pilot's fail light or any failure latches.

11-177. Failure of this test will report the below code.

79 Jammer Delay Calibration Failed.

Unlike the other calibration tested by BIT, Jammer Delay Calibration is not reattempted by BIT after a failure, since Jammer Delay Calibration can be done only in concert with, and at the initiation of the ICS.

11-178. LIMITER CALIBRATION TEST. This test tests IF Limiter Calibration passed an attempt to recover in case of failure. If the last execution of Limiter Calibration passed, nothing is done. If it failed, but the last execution of Gain and VCO Calibrations passed, a failure report is issued.

11-179. Failure of this test will report the below code.

108 Limiter Calibration failed.

11-180. LOW-BAND TEST. This test verifies the ability of low-band path to pass a signal. A dwell is done using the low-band BIT oscillator in LRU-3 as the source signal. The signal is routed through the C/D amplifier, into the channel A path leading out of LRU-3 over to LRU-6, through the low-band up-convert oscillator, into the Channel B Mode II, out of LRU-6, and back into LRU-3, using the medium-bandwidth mode.

11-181. The dwell time for this dwell allows six pulses to come in. If video data is received for at least four of these, the signal path is considered to be intact.

11-182. If less than four pulses are received for this dwell, the Mofified Low-Band Diagnostic Test is done to isolate where the failure is (LRU-2, LRU-3, or LRU-6).

11-183. The failure report for this test is only issued if the Frequency Coverage Test at the standard frequency (which uses the same Mod II filter as the up-converted BIT oscillator signal) passed for both channels, indicating that the failure is in the low-band component, either in LRU-3 or LRU-6.

11-184. Failure of this test will report the below code.

16 No signal in low-band test.

11-185. LRU-9 TEST. This test tests presence of Manchester link to LRU-9. A CAW 23 and a CAW 25 are issued to read the system flag word. If the LRU-9 bit in this word indicates presence of the Manchester link, the test passes. Otherwise, the test fails.

11-186. Failure of this test will report the below code.

70 No Manchester link to LRU-9 no diagnostic required.

1-187. NOTCH TEST. This test will test the LRU-3 Video Processor Notch Invocation and the Two Channel Notch Filters. The tests or dwells are done at three Intermediate Frequencies for each Channel A and B. The signal source originating in the LRU-6 is the Variable Picket Generator. The first dwell is done at the exact center of the LRU-3 IF band. Two additional dwells require the test frequency shifted ±200 from the IF center and is accomplished by tuning the Band I VCO.

11-188. The algorithm includes an amplitude test for each of the channels to determine if there is sufficient amplitude to assure the minimum Notch attenuation to the signal. This is accomplished by comparing signal amplitude to the receiver threshold. The difference must be an amount equal to or greater than the specified Notch Filler depth. The Frequency Rate Histogram has both limits enabled (i.e., Notch invocation is enabled), and threshold set to an initial 15. Dwell time would allow greater than 35 pulses to be received. It is expected that the Notch function will be invoked and block or attenuate the signal after nine pulses and that the Notch invovation flag will be set.

11-189. If no signals are processed and if more than nine pulses are received, or if no Notch invocation flag is set, a failure report is issued indicating the LRU-3 as the faulted unit.

11-190. The test is done in both Channels A and B. The Channel B test is attempted even if the Channel A test failed.

11-191. This test is not done if the Frequency Coverage Test did not receive a signal.

11-192. Failure of this test will report one or more of the below codes.

80 No signal seen in Channel A.
81 More than nine pulses received in Channel A.
82 No notch invocation flag in Channel A.
83 No signal seen in Channel B.
84 More than nine pulses received in Channel B.
85 No notch invocation flag in Channel B.
109 Notch, less than 9 pulses Channel A.
112 Notch, Less than 9 pulses Channel B.

11-193. ONE-MILLISECOND INTERRUPT TEST. This test tests that the 1-ms interrupt fires and that it can be enabled and disabled. With the 1-ms interrupt enabled and unclocked via the interrupt mask, and with the interrupt vector set to use a BIT counting routine rather than the usual interrupt handler, the code waits for about 1.25 ms. If an interrupt hasn't fired by the end of this time, a failure report is issued.

11-194. The 1-ms interrupt is then disabled and the code waits again for a slightly longer period of time. If the interrupt fires during this time, a failure report is issued.

11-195. At the conclusion of the test, the interrupt mask and 1-ms interrupt vector are restored to their original values.

11-196. Failure of this test will report one or more of the below codes.

93 1 ms interrupt doesn't fire when enabled.
94 1 ms interrupt fires when disabled.

11-197. RAM TEST. This test verifies proper functioning of the system's RAM. Specifically, the abilities to write into RAM and to retrieve data from RAM are tested for each RAM location in the system. The 80K of system RAM are divided into twenty 4K blocks. One 4K block is tested in each BIT segment; therefore, since a BIT segment is executed every 4 seconds, all of RAM is tested once a minute.

11-198. For each 4K block under test, the RAM Test sequentially tests each of its memory locations individually by saving its contents, writing a test pattern into it, retrieving its contents, verifying that its contents equal the test pattern, and restoring its original contents.

11-199. Not retrieving the correct test pattern from any location constitutes a RAM test failure. Should this occur, a failure report is produced indicating the 4K block containing the failed location, the test pattern that was used, and the pattern that was retrieved.

11-200. On successful completion of the test for a 4K block, counters are set to continue with the next block during the next BIT segment. On a failure, however, the counters are set to retest the failed block during the next segment.

11-201. The test patterns used are the one word, alternating bit patterns 5555 and AAAA, which are automatically selected alternately at the beginning of a complete RAM Test cycle.

11-202. Failure of this test will report the below code.

03 Retrieved contents not equal to test pattern.

11-203. SCREEN PROCESSOR HISTOGRAM TEST. This test tests for proper invocation of Screen Processor limit histograms. This test consists of a sequence of four dwells, all done at the standard frequency in medium bandwidth, in Channel A, using the fixed picket as the signal source and with the attenuation value derived during the Coarse CW Test.

11-204. This tests is only done if VCO Calibration passed. Furthermore, no failure reports are issued unless the Frequency Coverage Test for the standard frequency in Channel A passed, indicating that the signal path is intact. To maintain the test's histogram dependency sequence, the test will continue with the next dwell even when a step fails.

11-205. Before the test begins, a CAW 12 with value 070 is issued to clear limit histogram 0, which is used by this test (and is never used for S1 dwells which might still be active). The four dwells are then executed as follows: Test that when the RF and DF histograms are both enabled, the number of pulses is limited at 15. This is tested by doing one dwell with a long dwell time (enough for over 30 pulses). If the number of pulses received from this dwell is less than 15, or more than 15 plus some tolerance, the test fails.

11-206. Since a possibly unavoidable amplitude rise in one of the pulses would invoke hill climbing and reset the histogram, the tolerance added to the upper limit is currently set to another 15. This allows for hill climbing being invoked on as late as the last pulse.

11-207. Histograms are not cleared after this dwell to allow for the next test.

11-208. Test that after the RF and DF histograms have been invoked, hill climbing will allow more pulses to come in. This is done by repeating the first dwell, only this time turning on the 20-dB IF preamplifier to cause an amplitude rise and triggering the hil-climbing algorithm. If more pulses are received in video data (current implementation is satisfied with at lease one), the test passes.

11-209. The results of this dwell are not tested if the first dwell test did not pass.

11-210. Since it is important for the next dwell that the histograms have reached their limit in this dwell, this

dwell is done with a dwell time long enough for 45 pulses, or enough for two additional full hill climbing cycles each enabled on the last pulse of a group of 15.

11-211. Again the histograms are not cleared after this dwell to allow for the next test.

11-212. Test ability to bypass limit histogram invocation. This is done by repeating the previous dwell, but with RF and DF histogram bypass enabled. Dwell time is set to allow as many as 40 pulses into video data. If at least 32 pulses are received, the test passes.

11-213. Limit histograms are cleared after this dwell.

11-214. Test invocation of DF histogram alone. This is an eight-step auto-increment dwell around the standard frequency with a dwell time of seven pulses per step. The VCO tuning values for each step are forced to the value needed to see the center frequency. This guarantee receiving pulses in every step of the dwell, but with eight different RF tags due to the auto-increment stepping. Since all pulses will have the same DF, however, this should cause the DF histograms to be invoked by itself.

11-215. The DF histogram is invoked on the seventh RF associated with that DF. From then on, it should only allow in one pulse per new RF. Thus, the test's dwell is expected to result in six groups of RF tags containing seven pulses each and two more groups containing one pulse each.

11-216. There are two problems that can contribute to failure of this test, however, even though the DF histogram is functioning properly. The first is slight RF spreading from the fixed picket; this looks like a new RF to the DF histogram. Because of this, current test tolerances only test the first three of the first six groups of pulses.

11-217. The second problem is a slight amplitude rise during one of the steps that triggers the hill-climbing algorithms and resets the DF histogram. To prevent this before the test dwell, a preliminary dwell is done with a very short dwell time, with zero attenuation and without clearing histograms afterwards. This sets the amplitude level associated with the histograms to an abnormally high value; any slight rises in amplitude at lower levels during the test dwell will then not cause hill climbing to be invoked.

11-218. Other test tolerances are: passing with at least two pulses on the first steps (rather than demanding the full seven), and allowing two pulses (rather than one) on the last steps.

11-219. Both dwells done for this test have the RF bypass enabled to be sure the DF histogram is counting all RFs that are present.

11-220. The test dwell's tuning words include a parameter set to produce group statements for each step that receives multiple pulses. These group statements will be tested by the next execution of the Group Statement Test.

11-221. Failure of this test will report one or more of the below codes.

39 Too few pulses seen, appears that RF and DF histograms are being invoked too early.
40 Too many pulses seen, appears that RF and DF histograms are being invoked too late.
41 Hill-climbing algorithm not allowing in more pulses of amplitude rise.
44 RF and DF histogram bypass not functioning.
45 Early increment step received one or less pulses, appears that DF histogram is invoked too early.
46 The seventh or eighth increment step received more than two pulses, appears that DF histogram is invoked too late.

11-222. SCREEN PROCESSOR PARAMETER LIMITS TEST

11-223. This test tests the ability of Screen Processor to implement accept and reject screens. The functioning of pulse buffer reject function is also tested. Using the 131T oscillator in the LRU-3 as the source signal, it is routed into Channel B in wideband where two dwells are done.

11-224. This first dwell is done with four accept screens and a reject screen. Each of the first three accept screens has one parameter (RF, PW, and DF, respectively) set improperly for receiving the souce signal, while the fourth accept screen has all parameters set wide open. When the dwell is done, only the fourth accept screen will allow the data through. Screen threshold is set to zero. Dwell time is long enough to receive at least a dozen pulses. It is expected that the dwell will produce at least six pulses, all containing screen ID 4 (indicating that the fourth accept screen accepted the pulses). If this is not the result, a failure report is issued.

11-225. For the second dwell, the fourth accept screen

is changed to a reject screen. No pulses should be received in video data for this dwell; if there are any, a failure report is issued.

11-226. For the third dwell, the fourth screen is restored to an accept screen and the screen threshold is set to ten counts higher than the average amplitude seen in the first dwell. No pulses should be received in video data for this dwell; if there are any, a failure report is issued.

11-227. If either of the first two dwells fail, the subsequent portions of the test are omitted.

11-228. These dwells' tuning words also include a parameter set, using the dummy dwell ID 0 and a detection threshold of two pulses. This would cause a group statement to be produced when at least two pulses are accepted by an accept screen. However, all accept screens have the "pulse buffer reject" bit set, which should prevent any pulses from being sent to the group statement pulse buffer. If the group statement for this test is actually produced, the Group Statement Processor software will set a special flag that is tested during the Critical Flags test.

11-229. This test is not done if the Threshold Test did not see a signal.

11-230. Failure of this test will report one or more of the below codes.

55 No pulses received in first dwell.
56 Incorrect screen ID in first dwell.
57 Pulses received in second dwell.
58 Pulses received in third dwell.

11-231. SPU TEST. This test tests for proper operation of the SPU paths and their associated operations. A sequence of seven dwells, each testing a different function is done in both Channels A and B, as follows:

a. Tests for no noise on the baseband SPU line. This is done by a dwell without a source signal while tuned to a baseband frequency and testing the SPU amplitude. The SPU Enable Low switch is enabled. The 20-dB amplifier in the IF path is turned on to ensure that threshold will be crossed and video pulse reports will be received. RF and SPU bypasses are enabled, threshold is set to zero and the video processor pulse-width limits are opened to ensure that these noise pulses are all allowed into the video data. If the average SPU amplitude is below ten counts, no signal is considered to be present and the test passes. If the amplitude is above ten counts, a failure report is issued indicating which channel failed and what SPU amplitude was received.

b. Tests that the baseband SPU line can pass a signal. This time the dwell is done, again tuned to a baseband frequency, but with the fixed picket on, the 20-dB amplifier off, RF bypass disabled, and VP pulse-width limits closed. The test passes only if the average SPU amplitude is now above ten counts. If the amplitude is below ten counts, a failure report is issued indicating the failed channel and the received SPU amplitude.

c. Check for no noise and for the ability to pass a signal on the high-band SPU line. These tests are identical to tests a and b, only this time the receiver is tuned to a high-band frequency and the SPU Enabled High switch is enabled.

d. Tests that the SPU offset values can be set to accept pulses. This involves repeating the dwell of test e., but with SPU bypass disabled and the SPU offset numbers set to their most negative values. The dwell time for the dwell is long enough for six pulses. If at least four pulses are seen, the test passes. If less pulses are seen, a failure report is issued indicating the failed channel.

e. Tests that the SPU offset values can be set to reject pulses. The difference between the Superhet and SPU amplitude reports received in the previous dwell is used to determine the SPU offset value that should cause pulses from the signal to be rejected. SPU bypass is still disabled. If no pulses are received when the dwell is done, the test passes. Otherwise, a failure report is issued indicating the failed channel.

f. Tests the SPU bypass function. The dwell of step f is repeated with SPU bypass enable. If at least four of the six possible pulses are received, the test passes. Otherwise, a failure report is issued indicating the failed channel.

11-232. When any test failures occur, all the subsequent tests are not run. It is particularly significant that if a Channel A test fails, no Channel B test is done. The only exception is that if either of the baseband tests (a and b) fail the high band tests (c through f) will still be attempted. If either of the tests for no noise test (a or c) fails, the current implementation of BIT is not able to fault isolate the source of the noise to a particular LRU. The failure will

be arbitrarily attributed to the LRU-6, since this box has been found to cause this failure more frequently than any other. If either of the tests for signal tests (b or d) fail, the SPU Diagnostic Test will be done.

11-233. Failure of this test will report one or more of the below codes.

23 Noise on SPU baseband path.
24 No signal on SPU baseband path.
25 Noise on SPU high-band path.
26 No signal on SPU high-band path.
33 SPU offset values can't be set to accept.
34 SPU offset values can't be set to reject.
35 SPU bypass not functioning.

If any of the signal path tests (a through d) receive no pulses, this is indicative of a Superhet path failure that will be detected by other tests (particularly Frequency Coverage). In such a case, no failure is reported by the SPU Test and the remaining tests for that channel are omitted.

11-234. STROBE DELAY CALIBRATION TEST. This test tests the Strobe Delay Calibration passed and attempted to recover in case of failure.

11-235. If the last execution of Strobe Delay Calibration passed, nothing is done. If it failed, the calibration is redone. If it fails again, a failure report is issued.

11-236. The failure report will not be issued unless the Frequency Coverage Test at the standard frequency passed in both channels (indicating intactness of the signal paths). Also, the failure report will not be issued if any of the previous executions of gain, VCO, limiter, or discriminator calibrations failed.

11-237. The failure report diagnostic data includes the strobe delay values produced by the last calibration prior to this test.

11-238. Failure of this test will report one or more of the below codes.

72 Strobe delay calibration failed, although the variable picket could be seen.

73 Variable picket could not be tuned (its signal not seen).

11-239. THRESHOLD TEST. This test tests the ability of amplitude rate histogram to raise the threshold setting, ability to bypass threshold reports, and ability of threshold to block pulses. Three dwells are done, all using the BIT oscillator in the LRU-3 as the source signal, routing it into the wideband IF path in Channel B.

11-240. In the first dwell, the frequency rate histogram is shut off, the amplitude rate histogram is in mode 1 (which will cause threshold raising when 8 pulses have been received within 300 μs), and the threshold is set to 15. Dwell time would allow 30 pulses. The dwell is expected to cause eight pulses to be received in video data, one of which should have the threshold raised flag set. If less than eight pulses are seen, a failure report is issued and the LRU-2 Rebound Test will be executed as a diagnostic. If the threshold raised flag is not present, a failure report will also be issued.

11-241. The second dwell is identical to the first only with the Bypass Notch/Threshold Report in the Screen Processor Control word set. As in the first dwell, if less than eight pulses are seen, a failure report is issued and the LRU-2 Rebound Test will be executed as a diagnostic. But this time, a failure report will also be issued if the threshold raised flag is present.

11-242. For the third dwell, the threshold is set to 10 dB above the average amplitude level seen in the second dwell. This should prevent any pulses from coming in. If any do, a failure report is issued.

11-243. The second and third dwells are not attempted if the first one failed. The third is not attempted if the second one failed either.

11-244. Failure of this test will report one or more of the below codes.

48 No signal in first or second dwell.
49 No threshold raised flag in first dwell.
50 Signal received with amplitude below threshold in third dwell.
51 Threshold raised flag in second dwell.

11-245. TRACKER TEST. This test tests the ability to open tracker windows of specified durations at specified times.

11-246. This tests consists of two parts. The first part tests out the tracker hardware. The second part tests out the pulse-width limit function of the Video Processor. The dwell used in the first part of the test is enabled again via the P-BUS, with just one change: the Video Processor pulse-width limits in the tuning words are closed. No pulses should then be passed out of the Video Processor. If any pulses are received, a failure report is issued.

11-247. A Channel A dwell at the standard frequency is enabled by outputting the tuning words as tracker data via the P-BUS. The input signal (fixed picket) is chopped using the VP Pulse Mode which modulates the signal On for 200 ns and Off for 1.4 µs. Two tracker windows are opened 100 µs apart, each about 6 µs wide. The TOA's of the input video pulses should reveal two groups of two or three pulses each with a 100 µs gap between the two groups and 1.6 µs between pulses within a group. If no pulses are received, a failure report is issued if the Frequency Coverage Test in Channel A at the standard frequency passed (indicating that the signal path is intact). If pulses are received but the TOA's don't have the expected pattern, a failure report is always issued. A failure report is also issued if either window failed to produce an end-of-window interrupt.

11-248. Failure of this test will report one or more of the below codes.

36 No end-of-window interrupt.
37 Fails to acquire signal.
38 Incorrect pulse pattern.
47 Not limited on PW in video processor.

11-249. VCO CALIBRATION TEST. This test tests if the VCO calibration passed and attempt to recover in case of failure. If the last execution of VCO calibration passed, nothing is done.

11-250. Similarly, if no Channel B Frequency Coverage Test step passed (indicating a failure in Channel B signal path), nothing is done. Otherwise, an initial VCO calibration is reattempted. If the VCO calibration fails a second time and the previous gain calibration has passed, a failure report is issued.

11-251. Failure of this test will report the below code.

74 VCO calibration failed.

11-252. VIDEO PREPROCESSOR TEST. This test tests the ability of the Video Preprocessor to demultiplex a signal to its source antenna. Four dwells are done, one for each high-band antenna, using the variable picket as the source signal and operating in medium bandwidth. If the variable picket cannot be tuned in a particular channel, that channel's tests are not done. The input signal is put in chop mode, strobing for the desired antenna for each dwell and the Video Processor is set in the corresponding commutate mode. A DF screen is set up to only accept pulses coming from the desired antenna. Dwell time will allow six pulses. If at least four of these are received, the test passes.

11-253. If less than four pulses are received, then the results of the last strope delay calibration are examined. If the calibration failed, then no failure report for the Video Preprocessor Test is issued. Otherwise, the calibration is re-done and a Video Preprocessor Test failure report will be issued if the calibration still passes and if the Frequency Coverage Test at the standard frequency passed for the failed channel. The failure report will contain the strobe delay values that were active when the dwell first attempted.

11-254. Failure of this test will report one or more of the below codes.

27 No signal on either Channel A antenna.
28 No signal on either Channel B antenna.
29 No signal on antenna 1.
30 No signal on antenna 2.
31 No signal on antenna 3.
32 No signal on antenna 4.
100 Could not tune variable picket but variable picket saw signal.
101 Could not tune variable picket because variable picket did not see signal.

11-255. SYNCHRONOUS FAILURE CODES DESCRIPTIONS.

11-256. FATAL INTERRUPTS. A failure report is issued upon the firing of any interrupt that is stimulated by a system problem and that causes a cold system restart. Three interrupts fall into this class:

a. Dead-Man Timer Interrupt-fires whenever the DMT hasn't been reset for about 10 seconds and sets the LRU-2 latch whenever it fires twice within 20 to 25 seconds. If the OFP is executing properly and the computer is working properly, the DMT will always be reset before the interrupt can fire.

b. Memory Parity Interrupt--fires and sets the LRU-2 latch on an attempt to write into EEPROM or on an attempt to access nonexisting memory. If the OFP is executing properly and the computer is working properly, this event should never occur. If it does occur, the interrupt handler will do a computer BIT test before restarting the system.

c. Group Statement Pulse Buffer Overhead Interrupt--fires on a full group statement pulse buffer. If the OFP is executing properly, and the computer and Group Statement Processor are

working properly, the pulse buffer should never fill up.

11-257. The failure report for any of these interrupts includes the contents of the program counter at the time of the interrupt firing and the address of the last task invoking before the interrupt firing. These Interrupts will not set a fail latch.

11-258. Failure of this test will report one or more of the below codes.

01 Dead-Man Timer interrupt fired.
02 Memory Parity interrupt fired.
14 Group Statement Pulse Buffer Overload interrupt fired.

11-259. SCAN HANGUPS. A failure report is issued upon discovering an event that indicates improper functioning of the scan. Any of the below is considered such an event.

a. DMA-Out has been inactive for too long. Not being active means the scan has ceased tuning the receiver.

b. No S1 end of scan for too long. This indicates that something has interferred with the normal scan sequence.

c. Screen Processor doesn't become inactive when it should. This is tested four times (at beginning of calibration, beginning of BIT, end of section, end of break) when no more data is expected to be coming in and, hence, the Screen Processor should be idle. If it remains active, a dwell hasn't terminated when it should have.

11-260. The failure report for any scan hangup includes the starting addresses of the tuning words for the last two dwells enabled as well as the DMA-Out status (i.e., address of last word sent out) at the time the hangup was detected.

11-261. The recovery methods for the scan hangups differ, depending on the severity of the hangup. For DMA-Out being inactive when it should be active or Screen Processor not going inactive at the beginning of calibration or BIT, recovery involves just restarting the scan. For no S1 end of scan, and Screen Processor not going inactive at the end of a section or break, recovery involves doing a warm system restart. Scan hang-ups will not set a fail latch.

11-262. Failure of this test will report one or more of the below codes.

05 Scan hangup, DMA-Out has been inactive for too long.
95 No SI End of Scan.
96 DMA-Out active upon entering BIT
97 Screen Processor not idle upon entering Calibration.
98 Screen Processor not idle in section handler.
99 Screen Processor not idle in break handler.

11-263. TRAINING MODE INDICATION. This is not a system failure and will not cause latches to set or the fail light to go on. The report is merely a record of when the pilot entered or left training mode.

11-264. Failure of this test will report the below code.

15 Entered/Left training mode.

11-265. CI VIDEO IF DMA-out does not become inactive with (x) MS or the screen processor does not become idle with (3x) MS, a failure report will be produced and the system will go into a warm restart.

11-266. Failure of this test will report one or more of the below codes.

119 CI Video DMA active too long.
120 CI Video Screen Processor busy.

11-267. COINCIDENCE TEST. This test tests whether the coincidence function is rejecting all signals going through the channelizer. This test is invoked when a wide-bandwidth signal from an LRU-6 source cannot be seen, but it is known that the IF patches are intact. The only ambiguity, therefore, is between the signal source in LRU-6 and the Channelizer which may be rejecting all signals passing through it because an open filter is causing the coincidence flag to be set.

11-268. To resolve this ambiguity, this test performs a wide-bandwidth dwell using the BIT oscillator source in LRU-3, with the coincidence function set to reject. If the signal is not seen, there is an LRU-3 problem, and the LRU-2 Rebound Test is invoked to complete the failure isolation. If this signal is seen, there is an LRU-6 problem, and the LRU-6 Rebound Test is invoked.

11-269. This test is done in Channel B since it is stimulated by a discriminator calibration failure which is detected in Channel B.

11-270. IF TEST. This test tests the IF path in the LRU-3 to resolve fault isolation ambiguities concerning the signal path. This test is done when no pulses are received from an LRU-6 signal source in

medium-bandwidth.

11-271. The IF Test does a single dwell using the BIT oscillator in the LRU-3 as the signal source, injecting the signal directly into the LRU-3 IF patch in the wide-bandwidth mode. Dwell time allows up to a dozen pulses.

11-272. If at least six pulses with correct RF tags are received, the test passes; if not, the test fails.

11-273. If the test fails, the LRU-2 Rebound Test must be done next to determine whether the fault is in LRU-2 or LRU-3. If the test passes, the fault is either in LRU-6 or in the medium-bandwidth filter in LRU-3. The Medium Bandwidth Filter Test should be done next to resolve this ambiguity.

11-274. Two versions of the IF Test exist: one for Channel A failures, and one for Channel B failures. Note that since the BIT oscillator signal only enters the IF signal patch after the switch-amplifier-switch in LRU-3, this test is unable to properly identify a failure in the switch-amplifier-switch as an LRU-3 failure.

11-275. LRU-6 REBOUND TEST. This test tests the data links between LRU-6 and LRU-3 to resolve fault isolation ambiguity between LRU-6 and LRU-2/3. This test is done when it is not known whether the failure of an LRU-6 function is due to a failure of a component in that box, or the inability of the LRU-2/3 combination to send out its commands to the LRU-6.

11-276. The LRU-6 Rebound Test consists of two pats: a P-BUS Rebound Test and a DMA Rebound Test. In the P-BUS Rebound Test, patterns are rebounded through the LRU-3/6 interface in the LRU-3, in both rebound command and rebound data formats. If the received data isn't as expected, the test fails.

11-277. If the LRU-6 Rebound Test fails, the fault is either in the LRU-2 or LRU-3; if it passes, the fault is in the LRU-6. If it fails, the LRU-2 Rebound Test should be done next to resolve the LRU-2/3 ambiguity.

11-277. MEDIUM BANDWIDTH FILTER TEST. Determine whether the medium-bandwidth filter in LRU-3 is working to resolve a particular fault isolation ambiguity between LRU-3 and LRU-6. This test is done when no pulses are received from an LRU-6 signal source in medium-bandwidth, and it has already been determined that the fault is either in an LRU-6 function or in the medium-bandwidth filter in LRU-3.

11-278. The test repeats the medium-bandwidth dwell with the LRU-6 signal source that received no pulses, only this time with RF bypass enabled. If the signal is seen, the medium-bandwidth filter is not working. If, again, the signal is not seen, then an LRU-6 function is not working, and the LRU-6 Rebound Test is required for proper fault isolation.

11-279. Two versions of this test exist: one for Channel A failures, and one for Channel B failures.

11-280. MODIFIED LOW-BAND TEST. This test tests the low-band BIT source in LRU-3 to resolve fault isolation ambiguity between the low-band components of LRU-3 and LRU-6. This test is done when no pulses were received from the low-band BIT source in LRU-3, when the pulses were routed to LRU-6 along Channel A, through the low-band up-converter, and back to LRU-3 on Channel B. It is known that the Frequency Coverage Test for the corresponding baseband frequency path passed. Hence, the only candidates for failed components are the low-band up-converter and its associated switches in LRU-6, or the low-band BIT source, the C/D band amplifier, or low-band switches in LRU-3.

11-281. This test routes the low-band BIT source signal into the Channel A IF path in LRU-3. If pulses are received in video data from the signal, the failure is in the LRU-6 function, and the LRU-6 Rebound Test is done next. Otherwise, the failure is in the LRU-3 function and the LRU-2 Rebound Test is done next.

11-282. SPU DIAGNOSTIC TEST. This test tests the LRU-3 portion of SPU line to resolve SPU line fault ambiguity between LRU-3 and LRU-6. This test is done when there is a failure to receive data on the SPU line in both baseband and high band.

11-283. The SPU Diagnostic Test repeats the failed dwell, but with the LRU-6 signal source turned off and the SPU BIT source in LRU-3 turned on. This tests whether the LRU-3 portion of the SPU line can pass a signal. If the SPU amplitude received from this dwell is above a predetermined value, the test passes and the fault is in LRU-6. Otherwise, the test fails and the fault is in LRU-3. Since the SPU signal path is routed through LRU-2, a determination that LRU-3 is operational cannot be definitively attributed to the LRU-6.

11-284. LRU-3/LRU-3 SUPPLEMENTAL TESTS. This battery of tests, called the LRU-3 and LRU-3 Supplementary tests, are designed in such a way as to do a heirarchial approach to doing BIT. The hierarchy

begins with Initialization Bit fully testing the LRU-2, its interrupts, communication with the LRU-3, and interrupts from the LRU-3. When and only when, Initialization Bit is completed successfully are the LRU-3 and LRU-3 Supplementary tests done.

11-285. The LRU-3 test contains a closed loop structure that will not go into testing exotic functions of tne box, or functions in the LRU-6, until the basic LRU-3 test has passed, then the LRU-6 is included in the test loop. This ensemble of tests is called the LRU-3 Supplementary test. The tests are structured in a way that will introduce one new untested element into the loop at a time. This will allow the BIT to increase the ambiguity resolution performance.

11-286. The LRU-3/LRU-3 Supplemental Diagnostic is composed of Initialization Bit and LRU-3/LRU-3 Supplemental test Initialization Bit is discussed in greater detail in a separate section of this manual.

11-287. The LRU-3/LRU-3 Supplemental Tests are a group of tests designed to first test the LRU-3 using the LRU-3 signal source, then extend out to include testing of the LRU-6/LRU-3 path using the LRU-6 sources as input. The individual test routines that make up this group of tests are designed as basic tests to test out as much of the hardware (LRU-3 and LRU-6) as possible. The below is a list of the tests and the order in which they are done.

1. Functional/Operational checkout tests (LRU-3 only)
2. Low Band Signal Path Test I and II
3. Variable Picket Substitution Test (with CHB Atten/Amp Test)
4. Discriminator Crossing Test
5. Discriminator Flatness Test
6. Channel A Center Test (with CHA Atten/Amp Test)
7. Medium Band Path Low Signal Test
8. Medium Band Filter Log Amp Compliance Test
9. V.N.B. Isolation CW Path Test (with NB check)

11-288. This new diagnostic resides in the Failure Management Module (FM) and is called upon a failure of a detection test. If the diagnostic tests pass then the original fail code is processed. If, however, any of the diagnostic tests fail then a new fail code is produced from the test that failed and that fail code is processed. The copy of the original fail code is saved to diagnostic Word 3 of the current failure buffer being processed.

11-289. Not all fail codes produced cause the diagnostic to execute. Following is a description of the LRU-3/LRU-3 Supplemental tests.

11-290. LRU-3 TESTS:

11-291. LOG TEST CHA. This test tests the BIT oscillator in the LRU-3, its path to SW/FILTER/SW, IF path CHA, log video CHA, DF stare mode logic antenna 1, leading edge bypass pulse processing abilities in CHA, channellizer at one point (center tag +160), and LRU-2 communication with the LRU-3.

11-292. Failure of this test will report one or more of the below codes for Antenna 1.

121 Minimum number of pulses not received.
123 RF Tag not within limits.
125 Average amplitude not within limits.
127 DF not within limits.

11-293. LOG TEST CHA Test DF stare mode antenna 3 into the test path. Also records amplitude A1 for threshold setting for next test.

11-294. Failure of this test will report one or more of the below codes for Antenna 3.

129 Minimum number of pulses not received
131 RF Tag not within limits
133 Average amplitude not within limits
135 DF not within limits

11-295. AMBIENCE TEST CHA. Test the system for ambience recognition. Declare a no data condition with CW source and no leading edge bypass mode.

11-296. Failure of this test will report the below code.

137 Pulses were received - Channel A

11-297. PULSE TEST CHA. This test tests the system's ability to see real pulses (containing leading edges) produced from LRU-3 with the threshold 4db below recorded amplitude A1. Test BIT CHOP mode that modulates SW/FILTER/SW (CAW A). Preliminary threshold setting 4db below signal amplitude.

11-298. Failure of this test will report one or more of the below codes.

139 Minimum number of pulses not seen
141 RF Tag not within limits

143 DF not within limits
145 Average PW not within limits

11-299. THRESHOLD TEST CHA. This tests the system's ability to set a threshold in CHA.

11-300. Failure of this test will report one or more of the below codes.

149 Pulses were received

11-301. SPU OUTPUT TEST. Ensure there is no noise on the SPU line CHA. Note: This is the only time during the LRU-3 Test where an LRU-6 failure is declared.

11-302. Failure of this test will report one or more of the below codes.

151 No pulse data received - Channel A
153 SPU Amplitude seen - Channel A

11-303. CHECK SPU BIT SOURCE. Ensure the SPU BIT source is operational in CHA. (DC Offset).

11-304. Failure of this test will report one or more of the below codes.

155 No pulse data received
157 SPU amplitude < Reference Amplitude

11-305. SEE DATA WITH SPU BIT SOURCE ON. Ensure the SPU OFFSET function is operational in CHA in which a pulse is recognized with the SPU BIT Source on and SPU offset value set to most negative value.

11-306. Failure of this test will report one or more of the below codes.

159 Minimum number of pulses not seen
161 Average RF Tag not within limits

11-307. REJECT DATA WITH SPU BIT SOURCE. Test the Video Processor's ability of killing pulses based on spurious signals (Spurious signal in this case meaning the SPU BIT and SPU offset at its most positive value combined).

11-308. Failure of this test will report one or more of the below codes.

163 Pulse data was received

11-309. SPU BYPASS TEST CHA. This test tests the SPU bypass function of the system Channel A.

11-310. Failure of this test will report one or more of the below codes.

165 Minimum number of pulses not seen
167 RF Tag not within limits

11-311. LOG TEST CHB. This test tests the BIT Oscillator path to SW/FILTER/SW in the LRU-3, IF path CHB, log video CHB, DF stare mode logic antenna 2, leading edge bypass pulse processing abilities in Channel B.

11-312. Failure of this test will report one or more of the below codes for Antenna 2.

122 Minimum number of pulses not received
124 RF Tag not within limits
126 Average amplitude not within limits
128 DF not within limits

11-313. LOG TEST CHB. This test tests DF stare mode antenna 4 into the test path. Records amplitude B2 for threshold setting for next test.

11-314. Failure of this test will report one or more of the below codes for Antenna 4.

130 Minimum number of pulses not received
132 RF Tag not within limits
134 Average amplitude not within limits
136 DF not within limits

11-315. AMBIENCE TEST CHB. This tests the system for ambience recognition (Don't call ambience a pulse in leading edge bypass mode).

11-316. Failure of this test will report the below code.

138 Pulses were received - Channel B.

11-317. PULSE TEST.This tests the system's ability to see real pulses produced from LRU-3 with the threshold 4db below recorded amplitude B2. Tests BIT CHOP mode that modulates SW/FILTER/SW (CAW A).

11-318. Failure of this test will report one or more of the below codes.

140 Minimum number of pulses not seen
142 RF Tag not within limits
144 DF not within limits
146 Average PW not within limits

11-319. SPU OUTPUT CHB TEST. This test ensures there is no noise on the SPU lines in CHB.

11-320. Failure of this test will report one or more of the below codes.

152 No pulse data received - Channel B
154 SPU Amplitude seen - Channel B

11-321. CHECK SPU BIT SOURCE CHB. This test ensures that the SPU BIT source is operational in CHB.

11-322. Failure of this test will report one or more of the below codes.

156 No pulse data received - Channel B
158 SPU Amplitude < Reference Amplitude

11-323. SEE DATA WITH SPU BIT SOURCE ON CHB. This test tests to ensure that the SPU OFFSET function is operational in CHB in which a pulse is recognized with the SPU BIT Source on and SPU offset value set to the most negitive value.

11-324. Failure of this test will report one or more of the below codes.

160 Minimum number of pulses not seen - Channel B
162 Average RF Tag not within limits - Channel B

11-325. REJECT DATA WITH SPU BIT SOURCE CHB. This test tests the Video Processor's ability of killing pulses bases on spurious signals (spurious signal in this case meaning the SPU BIT and SPU offset combined).

11-326. Failure of this test will report the below code.

164 Pulse data was received

11-327. SPU BYPASS TEST CHB. This test tests the SPU bypass function of the system Channel B.

11-328. Failure of this test will report one or more of the below codes.

166 Minimum number of pulses not seen - Channel B
168 RF Tag not within limits - Channel B

11-329. C/D AMP TEST. This test tests the C/D amplifier (low gain) and C/D path from BIT OSC to the SW/FILTER/SW.

11-330. Failure of this test will report one or more of the below codes.

169 Minimum number of pulses not seen.
170 Average amplitude not within limits.

11-331. LOGS ONLY TEST. This test tests that the noise source produces adequate power and records the magnitude of the threshold setting for next two tests.

11-332. Failure of this test will report one or more of the below codes.

171 Minimum number of pulses not seen.
172 Average amplitude not within limits.

11-333. SEE DATA WITH THRESHOLD SET TEST. This test tests the ability of the system to perceive the noise signal with threshold set.

11-334. Failure of this test will report one or more of the below codes.

173 Minimum number of pulses not seen.
174 Average amplitude not within limits.

11-335. COINCIDENCE KILL TEST. This test tests the coincidence killing function of the video processor.

11-336. Failure of this test will report one or more of the below codes.

210 Pulse data was received.

11-337. LRU-3 SUPPLEMENTAL TESTS. LOW BAND SIGNAL PATH TEST 1. This tests the LRU-6 LB path into LRU-3. Uses the LRU-3 BIT OSC and positions the signal on the tested portion of the discriminator (center tag + 160 point) C/D amp still in low gain mode. Records amplitude for the next test. If this test fails, the LRU-6 rebound is done, thus resolving the ambiguity between the LRU-3 and LRU-6.

11-338. Failure of this test will report one or more of the below codes.

175 RF Tag out of limits (LRU-6 Fail).
176 RF Tag out of limits (LRU-3 Fail).
177 No attenuation (LRU-6 Fail).
178 No attenuation (LRU-3 Fail).
179 No 20db gain in amplifier.

11-339. LOW AND SIGNAL PATH TEST II. This test tests the C/D amplifier in high gain mode. (Computes the delta magnitude between low and high gain mode).

11-340. Failure of this test will report one or more of the below codes.

219 Low Band test amplitude not acceptable (LRU-6 Fail).
220 Low Band test amplitude not acceptable (LRU-3 Fail).

11-341. VARIABLE PICKET SUBSTITUTION. This tests tests the variable picket and CHB signal path from variable picket to the RF switch on 5A3 in the LRU-6. Signal path includes Mod VI, diplexer, band II amplifier, one Mod I path, one high-band mixer mode. This test also calls Attenuator/Amplifier Boot strap

Test CHB.

11-342. This test performs four tasks:

a. First detection of variable picket signal in the bandpass.
b. Second detection of variable picket signal in the bandpass.
c. Convergence of desired RF Tag
d. Switch/Amplifier/Switch Channel B amplifier test

11-343. This test is done by taking X amount of tuning steps at attenuation value N and sweep across the fundamental frequency range. If no signal is seen after all tuning steps are completed reduce attenuation. If no attenuation is left, conclude an LRU-6 failure. If the signal was seen verify the signal was indeed the variable picket and not noise by turning the picket off and doing an additional dwell. If a signal is still seen then this is actually noise and not the variable picket. At this point we want to reduce attenuation by X number of counts until there is a 10db delta of signal magnitude. Lower attenuation in 6db increments till there is a 10db magnitude delta.

11-344. Verify signal can be seen again somewhere else in the bandpass. Increment Variable Picket tuning value by 50 counts. If signal not seen move tuning value in the other direction decrement tuning value by 100 counts. If signal is not seen do some diagnostic work. Restore original tuning value and increment VCO by 50 counts. If signal is seen, LRU-6 failure. If signal not seen, LRU-3 failure.

11-345. COVERAGE ON DESIRED RF TAG: Interpolate ideal Variable Picket tuning value using previous tag, tuning value, current tag, tuning value. Do a dwell. Continue process for X number of tries or a hit (center tag + 160 +/- tolerance) whichever comes first. If no hit made, retune to previous value, compute delta between previous and ideal tag. Subtract delta from VCO. Now try for a hit by moving VCO. If a hit made, LRU-6 failure. If no hit made, LRU-3 failure.

11-346. Failure of this test will report one or more of the below codes.

180 Noise.
181 No variable picket seen.
182 Attenuator could not reduce signal magnitude.
183 Variable picket not movable.
184 Discriminator.
185 Discriminator convergence error.
186 Variable picket convergence error.

11-347. ATTENUATOR/AMPLIFIER BOOTSTRAP TEST CHB. This tests the amplifier in the SW/AMP/SW and the functionality of the attenuator in CHB.

11-348. Do SWITCH/AMPLIFIER/SWITCH Channel B amplifier test if a hit with correct tag was made (center tag + 160 +/- tolerance). Set SWITCH/AMPLIFIER/SWITCH to gain mode. Do a dwell and take a data sample. Verify if a valid gain +/- tolerance is present. If gain not valid, report an LRU-3 failure.

11-349. Remove SWITCH/AMPLIFIER/SWITCH from gain mode. Take a data sample and adjust attenuation accordingly until reported magnitude is equal to or greater than the magnitude reported with the switch/amplifier/switch in gain mode. If unable to adjust attenuation accordingly, report an LRU-6 failure.

11-350. Failure of this test will report one or more of the below codes.

187 20 DB amplifier error.
217 Variable picket substitution test attenuator failure.

11-351. DISCRIMINATOR CROSSING TEST. This test tests the eleven discriminator crossing points by using the variable picket and moving the VCO. This test will determine that each discriminator filter is alive and test the VCO at many points. (This test exercises operability of CHB). If this test fails, the VCO is set to value that was tested successfully and the variable picket is modified to stimulate each discriminator filter. This diagnostic will resolve the VCO/Discriminator ambiguity.This test tests that the variable picket tuning value has been determined by the picket substitution test. The VCO has been open loop tuned yielding a tag (center tag + 160 +/tolerance). The tag must be moved from center tag + 160 to center tag + 200 to center tag + 250. Center tag + 250 is the first ideal RF Tag. The ideal RF Tag is decremented down to 0 in steps of 50. The actual change in VCO shall be computed via interpolation. The observed RF Tag of each discriminator crossing and the VCO tuning value used are saved in a discriminator crossing table. If an RF Tag is not within limits a discriminator crossing diagnostic is done. The VCO will remain constant and the variable picket will be moved in steps of 50. The actual change in the variable picket tuning value shall be computed via interpolation. If the RF Tags are not

within limits then there is an LRU-3 failure. If the RF Tags are within limits then there is an LRU-6 failure.

11-352. Failure of this test will report one or more of the below codes.

188 Discriminator Crossing failure.
189 Discriminator good, VCO bad.
198 Variable Picket Fail.

11-353. DISCRIMINATOR FLATNESS TEST. This test will test the center of the discriminator for monotonicity and flatness. Diagnostic for this test sets the VCO to a value that was tested successfully and modifies the variable picket to simulate the same test. This diagnostic will resolve the LRU-3/LRU-6 ambiguity. Two frequency auto-increment (FAIM) dwells are done. Each dwell covers 25 count steps. The dwell time allows 3 pulses to be collected on each step. The variable picket remains fixed. Each reported RF tag is examined. Small deviations (+/- tolerance) are tolerated so as not to be too sensitive.

11-354. If RF tags not within limits then a diagnostic is done. The VCO tuning value remains constant and the variable picket will proceed upward in 50 count steps. If RF tags within limits then, LRU-6 failure. If RF tags are not within limits, LRU-3 failed.

11-355. After all tags have been examined test for an upward trend in the tags. The difference between the last tag and first tag must be between 10 - 40. If failed upward trend do the diagnostic mentioned above.

11-356. Failure of this test will report one or more of the below codes.

190 VCO fail
191 Discriminator fail

11-357. CHANNEL A CENTER TEST. This test is designed to test CHA WB path from the variable picket to SW/FILTER/SW in the LRU-3. (SW/FILTER/SW back has been tested in WB).

11-358. The test performs three tasks:

a. Verifies an LRU-6 signal can be seen in Channel A.
b. Verifies the SWITCH/AMPLIFIER/SWITCH of Channel A provides reasonable gain.
c. Verifies the Channel A attenuator can produce at least as much attenuation as the switch/amplifier/switch provided gain.

11-359. Set up for Channel A. Tune variable picket. Start with maximum attenuation. Reduce attenuation by 5db until signal is present. If no signal present report an LRU-6 failure. If signal present verify reported center RF tag plus tolerance. Adjust attenuation and reduce signals magnitude by 6db. If RF tag not within limits report an LRU-6 failure.

11-360. Set switch/amplifier/switch to gain mode. Do a dwell and take a data sample. Verify if a valid gain is present (+/- tolerance). If gain not valid, report an LRU-3 failure.

11-361. Remove switch/amplifier/switch from gain mode. Take a data sample and adjust attenuation accordingly until reported magnitude is equal to or greater than the magnitude reported with the switch/amplifier/switch in gain mode. If unable to adjust attenuation accordingly, report an LRU-6 failure.

11-362. Failure of this test will report one or more of the below codes.

192 Channel A LRU-6 path, no signal.
218 RF tag not within limits.

11-363. ATTENUATOR/AMPLIFIER BOOTSTRAP TEST CHA. This test tests the amplifier in the SW/AMP/SW and the functionality of the attenuator in CHA.

11-364. Failure of this test will report one or more of the below codes.

193 Switch/amplifier/switch- CHA insufficient gain.
194 Failed Channel A attenuation.

11-365. MEDIUM BAND CHA/B PATH & LOW SIGNAL TEST.

11-366. This tests the functionality of medium band processing in Channel A/B and the center of the bandpass of the medium band filter.

11-367. Failure of this test will report one or more of the below codes.

195 Center RF or no signal CHA.
196 Center RF or no signal CHB.

11-368. MB FILTER 7 LOG AMP. COMPLIANCE TEST CHA/B. This test tests the shape of the CHA/B ME filter and ability of the log video CHA/B to traverse a specified range.

11-369. Failure of this test will report one or more of the below codes.

203 CHB magnitude not in range.
204 CHA magnitude not in range.
205 CHB MB slope or log mobility excessive magnitude difference.
206 CHA MB slope or log mobility excessive magnitude difference.
207 CHB Log mobility (stuck in I/0 state).
208 CHA Log mobility (stuck in I/0 state).

11-370. VERY NARROW BAND & CW PATH TEST. This tests the filter response of the VNB filter for width and continuity. Tune the variable picket to +8 counts from the center. Set up for VNB. Do a 16 step frequency auto-increment dwell where the step size is -1 count. Expect to see data on 1 to 5 steps. If no data seen at all an LRU-3 failure is reported. If data seen on more than 6 steps then SAW FILTER is too wide. Report an LRU-3 failure. If data seen, on more than one step, test that the step numbers are contiguous. If not contiguous, an LRU-3 failure is reported.

11-371. Failure of this test will report one or more of the below codes.

211 No data in Fine CW.
212 Fine CW too wide.
213 Split Fine CW.

11-372. NB CHECK TEST. This test verifies that a signal path exists and that the narrow band filter has enough rejection. Determine the first NB dwell RF by computing the mean of the FCW step numbers (VNB test) and subtracting 12 counts. Do a 3 step frequency auto-increment dwell with a -12 count step size. If no data, an LRU-3 failure is reported. If data seen on a single step, the test is complete. If data seen on more than one step the magnitudes must be examined. The rejection must be at least the minimum specified value. If data seen on more than 3 steps, then an LRU-3 failure is reported.

11-373. Failure of this test will report one or more of the below codes.

214 No data in Coarse CW.
215 Insufficient rejection.
216 Narrow Band excessive data.

11-374. Automatic BIT. Automatic BIT, which is done at the end of each high band RF scan, is a programmed function of the fixed BIT routine. During the BIT mode of operation, the computer does the BIT routine and if the computer fails to complete the routine within a specified time, a CPU FAIL signal is produced indicating a computer malfunction.

11-375. When the computer fails its self-test routine, a CPU FAIL signal is produced and transmitted to a logic circuit. The logic circuit output signal LRU 2 FAIL is applied to a gating circuit and an RWR NO-GO signal is produced. The RWR NO-GO signal is applied to the BCP and flight director adapter. The BCP, as a result, lights the RWR light and the flight director adapter tells the central computer that the RWR is off. Also, the computer transmits the control instructions word for LRU 3-NG, as computer output data. The computer demand and computer command address signals enable the data to be shifted out of the register and applied to a shift register. The computer command address is decoded and the FAILBIT control word is then applied to the shift register as an enable signal. The shift register, when enabled, applies the LRU 3-NG signal, and its output signal (LB RECEIVER/PROCESSOR FAIL) sets the low band receiver/processor UNIT FAIL indicator (black and white) and ASP fail indicator 5 (orange).

11-376. An address decoder and dead man counter monitors the COMPUTER DEMAND and COMPUTER COMMAND ADDRESS signals for computer self-test commands. If the computer fails to start a self-test cycle within 10 seconds of a previous cycle as determined by the dead man timer, the dead man control flip flops produce a BIT INTERRUPT signal to command a computer self-test cycle. If the computer fails to receive this command within the designated time, the dead man counter produces a LRU 2 FAIL signal. This signal causes a RWR NO-GO signal to turn on the BCP RWR light, and a LRU 3-NG signal to set the low band receiver/processor UNIT FAIL indicator (black and white) and ASP fault indicator no. 5 (orange). If the computer resumes normal operation, the BCP RWR light goes off, but the UNIT FAIL indicator and ASP fault indicator no. 5 remain set.

11-377. Automatic BIT of the low band receiver/ processor is done at the end of each RF scan period. The first step in the sequence activates the LO oscillator. The injection signals are applied to the A and B filters. Following processing of the injection signals, the resulting recovered video signals are evaluated. The signals are tested for discriminator accuracy, PW and threshold rejection and surface acoustic wave mode calibration. Other tests include mux rebound, low band antenna DC BIT, tone filter

BIT and computer BIT.

11-378. If a malfunction is detected during the processing and analysis of the BIT oscillator and test tone frequencies, the computer transmits the control instruction words for RWR NO-GO and LRU 3-NG, as computer output data. The computer demand and computer command address signals enable the data to be shifted out of the register and applied to a shift register. The computer command address is decoded and the FAIL BIT control word is applied to the shift register as an enable signal. The shift register, when enabled, applies the LRU 3-NG signal to a gate/driver circuit, and the output signal (LB RECEIVER/ PROCESSOR FAIL) sets the low band receiver/ processor UNIT FAIL indicator (black and white) and ASP fault indicator 5 (orange). The RWR-NG signal is also applied to a gating circuit and a RWR NO-GO signal is produced. The RWR NO-GO signal is applied to the BCP and flight director adapter. The BCP, as a result, lights the RWR light and the flight director adapter tells the central computer that the RWR is off. A failure of the low band antenna causes the computer to transmit the control instructions words RWR NO-GO and LRU 8-NG (LB ANTENNA FAIL).

11-379. Automatic BIT of the high band receiver is done at the end of the second high band RF scan and then after alternate high band RF scans. High band control instruction word 6 defines and controls BIT enable for the high band receiver. High band BIT is done by turning on and operating the BIT CAL oscillator, and monitoring READY, THERMUX, and ANTENNA STATUS signals. Also, a parity test is made on each incoming BH control instruction word. This result is sent back to the low band receiver/ processor, through the power supply, on the H-PARITY line. A parity failure causes the computer to retransmit that specific control instruction word. A second consecutive parity failure causes the computer to start its self-diagnostic routine.

11-380. The H-BIT MULTIPLEX signals are applied to a line receiver and its signal (MULTI) is then applied to a gating circuit. The computer transmits a computer command and computer command address for MULTI-OUT control, The signals are decoded and the MULTI-OUT control word is applied to the gating circuits. The MULTI-OUT control word enables the MULTI output data to be shifted through the gating circuits as SERIAL DATA. The SERIAL DATA is applied through a logic circuit to an output register. The data is shifted from the output register and sent to the computer. If a malfunction is detected, the computer transmits the control instruction words for the RWR NO-GO and LRU 6-NG. However, a failure of the high band antenna status causes the computer to transmit the control instruction words for RWR NO-GO and either LRU 7 L-NG (LF ANTENNA FAIL), LRU 7 R-NG (RF ANTENNA FAIL), LRU 5 L-NG (LW ANTENNA FAIL), or LRU 5 R-NG (RW ANTENNA FAIL).

11-381. Automatic BIT of the display unit is started after each time the cross symbol is produced. CRT intensity is disabled to prevent the test display from being illuminated. The BIT function includes monitoring the X POS and Y POS deflection voltages. The voltage monitoring circuits are on X-Y digital to analog converter module. A failure detected in the X POS or Y POS voltages causes a SWEEP FAIL signal to be produced and the display unit to be shut off. The SWEEP FAIL signal is applied to a logic circuit. The logic circuit, when enabled by a TEST FAIL signal, applies a signal (DISPLAY FAIL) to a differential amplifier. The amplifier output signal (DISPLAY FAIL) is applied, through the power supply, to a logic circuit in the low band receiver/processor. The LRU 9 FAIL signal, from the logic circuit, is sent to a shift register. Also, the lack of a DATA REQ signal at the logic circuit causes a NO DATA REQ signal to be produced. The NO DATA REQ signal is applied to the logic circuit resulting in an LRU 9 FAIL signal being produced.

11-382. The FLAGOUT control word defines and controls the monitoring for a display fail signal. At some point in the program the computer transmits a computer demand and computer command address for FLAGOUT control. The signals are decoded and the FLAGOUT control word is applied to the shift register and gating circuits. The FLAGOUT control word enables the LRU 9 FAIL signal to be shifted from the register as FLAGOUT DATA and through the gating circuits as SERIAL DATA. The SERIAL DATA is applied through a logic circuit to an output register. The data is shifted from the output register and sent to the computer. On arrival in the computer, the DISPLAY FAIL flag is set.

11-383. When the flag is set, the computer transmits the control instructions words for DISPLAY FAIL and RWR NO-GO, as computer output data. The computer demand and computer command address signals enable

the data to be shifted out of the register and applied to a shift register. The computer command address is decoded and the FAIL BIT control word is applied to the shift register as an enable signal. The shift register, when enabled, applies the LRU 9-NG signal to a gate/driver circuit and its output signal (DISPLAY UNIT FAIL) is applied to the ASP, setting fail indicator 49 (orange). The DISPLAY UNIT FAIL signal is also sent, through the power supply, to the display unit setting the UNIT FAIL indicator (black and white). The RWR-NG signal from the shift register is applied to a gating circuit and the output signal (RWR NO-GO) is applied to the BCP and flight director adapter. The BCP, as a result, lights the RWR light and the flight director adapter tells the central computer that the RWR is off.

11-384. A failure within the RWR, that does not fully satisfy the RWR NO-GO requirements, results in the output signal RWR NO-GO being produced for the period of the failed test segment. The malfunctioning LRU UNIT FAIL indicator may or may not be set, depending on the significance of the malfunction. This results in an intermittent flashing of the BCP RWR light, indicating degraded operation of the RWR system.

11-385. Continuous BIT. Continuous BIT of the power supply is done by a BIT routine within the unit. At initial turn on, 115vac, 400 Hz, 3Ø primary power is applied to the power supply module where it is rectified (See Figure 11-3). The BIT circuitry continuously monitors the rectified 115vac, 400 Hz, 3Ø for correct operating tolerance. The power supply BIT operates independent of all other power supply functions.

11-386. The 25 millisecond and 15 microsecond clocks are enabled. The output signals, 25 MILLIX and 15 MICROX, are synchronized and control programmable read only memory (PROM) circuits in which the BIT program is stored. The 25 MILLIX and 15 MICROX signals are applied to the address latch starting the BIT program. The 15 MICROX and 25 MILLIX signals are also synchronized and the sync output is applied to a counter and counter decoder circuit to provide enable signals if a failure has occurred.

11-387. The 15 MICROX signal enables the address latch and the address code is then applied to the PROM. The PROM output data is decoded and applied to select and enable either Channel A or B multiplexers. Also, the PROM provides amplifier gain signals (ER GAIN) to analog switches. The ER GAIN signals applied through the analog switches to the respective variable gain amplifier determine the tolerance level the circuit will approve when testing a specific voltage. Since the first test done is for a high voltage condition, the PROM provides a mode signal (V TEST) to comparators to indicate voltage test is in operation.

11-388. The PROM, on being addressed, and after selecting and enabling the multiplexers, sequentially tests the power supply output voltages for a high voltage or low voltage condition. The sampled output voltages, through the multiplexers, are applied to amplifiers and comparators for a comparator test of the voltages versus the programmed tolerance levels. If a high voltage or low voltage condition is not detected, the cycle is repeated. If a high voltage condition occurs, a high voltage (HV) fail signal is applied to logic circuits. The detected failure causes an LRU fail signal and, through gating, sets the PWR SUP indicator (black and white). The power supply fail signal is also applied to the ASP, through the low band receiver/processor, setting fail indicator 5 (orange). A POWER SUPPLY NO-GO signal is produced and applied to a gating circuit in the low band receiver/processor which applies an RWR NO-GO signal to the BCP and flight director adapter. The BCP, as a result, lights the RWR light and the flight director adapter tells the central computer that the RWR is off.

11-389. If a low voltage condition is detected, a low voltage fail signal (LV) is applied to a latch on BIT logic module and its output causes the PROM address to be changed. This puts the BIT program in a current testing mode through the V TEST signal. The PROM then starts a sequential test of the power supply load voltages for an overcurrent condition. Again, the sampled output voltages, through the multiplexers, are applied to amplifiers and comparators for a comparator test of the voltages versus the programmed tolerance levels. If a high current condition is detected, a high current signal (HV) is applied to logic circuits. The detected failure causes the PROM to produce an LRU fail signal and through gating sets both the UNIT FAIL indicator of the defective LRU and the related ASP fail indicator. If a high-current was not sensed during the high-current test, the logic circuits cause an LRU fail signal to set the power supply UNIT FAIL indicator and related ASP fail indicator.

11-390. Continuous BIT of the display unit includes

monitoring the CRT operating voltages. The CRT operating voltages monitored are cathode (K) voltage, control grid (GI) voltage, second control grid (G2) voltage, filament (FIL) voltage, and anode voltage. A failure detected in any of the CRT operating voltages causes the display unit to be shut off. The DISPLAY FAIL signal is applied through the power supply to a logic circuit in the low band receiver/processor. The LRU 9 FAIL signal is generated and sent to a shift register.

11-391. The FLAGOUT control word defines and controls the monitoring for a display fail signal. At some point in the program, the computer transmits a computer demand and computer command address for FLAGOUT control. The signals are decoded and the FLAGOUT control word is applied to the shift register and gating circuits. The FLAGOUT control word enables the LRU 9 FAIL signal to be shifted from the register as FLAGOUT DATA and then through the gating circuits as SERIAL DATA. The SERIAL DATA is applied through a logic circuit to an output register. The data is shifted from the output register and sent to the computer. On arrival in the computer, the DISPLAY FAIL flag is set.

11-392. When the flag is set, the computer transmits the control instruction words for DISPLAY FAIL and RWR NO-GO, and computer output data. The computer demand and computer command address signals enable the data to be shifted out of the register and applied to a shift register. The computer command address is decoded and the FAIL BIT control word is then applied to the shift register as an enable signal. The shift register, when enabled, applies the LRU 9-NG signal to a gate/driver circuit. The output signal (DISPLAY UNIT FAIL) is applied to the ASP, setting fail indicator 49 (orange). Also, the DISPLAY UNIT FAIL signal is sent, through the power supply, to the display unit setting the unit fail indicator (black and white). The RWR-NG signal from the shift register is applied to a gating circuit. The output signal (RWR NO-GO) is applied to the BCP and flight director adapter. The BCP, as a result, lights the RWR light and the flight director adapter tells the central computer that the RWR is off.

11-393. If a malfunction is detected during the initial 5 minute warm-up, by either continuous or automatic BIT, the failure is indicated by the BCP RWR light only. The unit fail commands to the LRU and ASP fault indicators are inhibited by the computer. If the malfunction clears itself, the RWR light goes out. If the malfunction remains past the 5 minute warm-up, the RWR fight stays on and the appropriate fault/unit fail indicator(s) will be set.

11-394. Manual Initiated BIT. Manually started BIT is activated by positioning the BCP system select switch to RWR and pressing the INITIATE switch. Upon activating the BCP INITIATE switch, a discrete signal (MANUAL BIT INITIATE) is applied to relay K1 in the low band receiver/processor. Also, the discrete signal is applied to a BIT control circuit. BIT control circuit provides a BIT REQUEST signal to a shift register.

11-395. The FLAGOUT control word defines and controls the monitoring for a MANUAL BIT INITIATE signal. At some point in the program, the computer transmits a computer demand and computer command address for FLAGOUT control. The signals are decoded on computer input data control module and the FLAGOUT control word is applied to the shift register and gating circuits. The FLAGOUT control word enables the MANUAL BIT INITIATE signal to be shifted from the register as FLAGOUT DATA and then through the gating circuits as SERIAL DATA. The SERIAL DATA is applied through a logic circuit to an output register. The data is shifted from the output register and sent to the computer. On arrival in the computer, the MANUAL BIT INITIATE flag is set.

11-396. When the flag is set, the computer transmits the control instruction words for doing the manual BIT routine (fixed BIT). Also, the computer transmits the control instruction words for BIT ACKNOWLEDGE and TONE ENABLE, as computer output data. The computer command and computer command address signals enable the data to be shifted out of the register and applied to a shift register. The computer command address is decoded and the DISCRETE control word is applied to the shift register as an enable signal. The shift register, when enabled, applies the TONE ENABLE signal to both the launch and caution tone generators as an enable signal. Also the BIT ENABLE signal is applied to the BIT control circuits. Its output signal (BIT ACKNOWLEDGE) is applied to a relay gate/driver actuating relay K1. With relay K1 held actuated, the BIT ACKNOWLEDGE signal is applied to the BCP causing the RWR light to flash for the period of the manually started BIT program (approximately 10 seconds).

11-397. **System Interface.** Refer to Figure 11-10.

11-398. RF Compatibility. Operation of the TEWS system depends on exploitation of the radio frequency environment. This environment includes emissions from the radar system. The CC provides communication between the TEWS and radar. This allows the RWR and ICMS to modify their performance and reduce reception of the radar. By showing desensitization value of the radar, the CC allows selection of level of RF compatibility to add to the radar modes (offensive), ICMS modes (defensive), or the weapon system modes (auto). This indicates when the ICMS is operating in the radar frequency region.

11-399. Radar/TEWS Interface. The TEWS tries to avoid reception of the radar as much as possible. The radar/TEWS interface provides radar predicted transmit channels and timing to the RWR on a direct remote terminal to remote terminal transfer. This data is sent to the ICMS by the CC, and using this, the RWR establishes the frequency screens. The ICMS modifies or raises receiver thresholds to limit reception of onboard radar transmissions. For those radar modes where the predictions are inaccurate, true frequencies and times are provided to the RWR so processing can prevent detection of radar.

11-400. Improved Ambiguity Resolution (IAR). The IAR improves the ability to resolve ambiguities for some threats in specific modes that were ambiguous with other emitters while still maintaining the system operational requirements document (SORD) requirements. Air Warfare Command updates the PFM to include acquisition radars that are known to be tied to a certain emitter. The SORD insurance module (SIM) enables/disables this ability.

11-401. RWR Rapid Ageout (RAO). The RAO improves ageout requirements for up to the highest five threats on the display while still maintaining SORD requirements. The following emitters defined in the PFM as RAO candidates are eligible: LORO, CONSCAN, TWS with less than maximum hole and TWS operator special. The RWR RAO is only applied to one beam of a multibeam emitter and must be enabled by the SIM. RAO is not applied to an emitter updated within the last second or if look through has been denied by the ICMS the SIM enables/disables this ability.

11-402. Improved DF Accuracy (IDF). The IDF is designed to improve direction finding (DF) ability of the system while maintaining the SORD requirements. The SIM enables/disables this ability.

11-403. SORD Insurance Module (SIM). The RWR has a SORD insurance module which makes sure the RWR meets the SORD requirements for threat detection, response time, and ageout. The IAR, RAO and IDF is done as long as they do not reduce the abilities of the RWR below the SORD requirements. Once the RWR cannot meet SORD requirements, RWR functions are limited to protect total RWR performance.

11-404. RWR Detail Aircrew BIT. The RWR detail BIT design provides detailed information regarding the severity of RWR performance degradation. If a failure has occurred that causes the fail lamp to illuminate, the RWR transfers the correct failure message to the CC. The definition and English readout of the RWR functional failure information is coded into the CC OFP. The CC requests updated RWR functional failures following an RWR indication that new failure information is available. The updated RWR detail status display is available for selection from the TEWS detail BIT display. The RWR functional failure data is downloaded on the DTM for display/printout from the AFMSS station. Table 11-3 provides a summary of RWR functional failure indications that can be reported on the RWR detail BIT display.

11-405. RWR Display Symbols. The RWR software provides situational awareness through visual and audio enhancements. Symbology highlights the latest threat detected, emitters in launch mode, threat changes from search to track, launch alert, and ICMS asset allocation.

11-406. RWR Missionized PFM (MPFM). Three combat MPFM and one RWR training mode are available. Pressing S14 on the MPCD changes to the available MPFM sent from the RWR. On TEWS display, the MPFM legend remains in view for three seconds after the RWR has been commanded to the PFM. With the RWR in training mode, the MPCD will indicate this by an encircled zero at top of TEWS display. When the RWR is in training mode, S14 allows scrolling between combat PFM legends, even though only one RWR training mode PFM will be invoked.

11-407. Central Computer. The central computer (CC) does computations for navigation, weapon delivery and

control, and display processing using information received from various sensors. This data provides the RWR with radar, TACAN, attitude, altitude, and velocities data required for computation of threat location. Data transfer between the CC and the mux buses is done by the I/O section. The CC provides basic clock signals to the I/O section which produces the timing signals required for operation of the mux buses.

11-408. The mux buses transmit digital data between the CC and the RWR. The CC is the master terminal and the RWR is the remote terminal. The RWR communicates with the CC only after the CC sends a select word to the RWR.

11-409. The H009 mux bus for the RWR consists of two channels, primary (BUS 1) and secondary (BUS 3). MUX BUS 1 and 3 communicate with the low band receiver/processor. The primary bus transmits the digital data between the CC and the RWR. The secondary bus provides a backup function if the primary mux bus fails. The CC calls the RWR with a select word. The select word contains the RWR address, parity information, and a transmit/receive command. The RWR communicates with the CC only after it receives the correct select word. If the select word indicates a command message, the RWR acknowledges receipt of the command by transmitting one data word back to the CC that is identical to the select word received. If the select word indicates a data message, the RWR can transmit or receive data words.

11-410. The 1553 MUX BUS consists of two channels, primary (BUS 5A), and secondary (BUS 5B). MUX BUS 5A and 5B communicate with the low band receiver/processor, part of the RWR. The primary bus transmits the digital data between the CC and the RWR. The secondary bus provides a backup function if the primary mux bus fails. The RWR provides its own reference clock which its synchronized by the transmitted CC words. There are three types of words: command, status, and data words. The command words control transmission and reception of the specified data by the RWR. The status words contain the operational status of the RWR. The data words contain parameter and discrete information. The RWR communicates with the CC only after it receives the correct command word. The RWR then transmits or receives data, depending upon the command word from the CC.

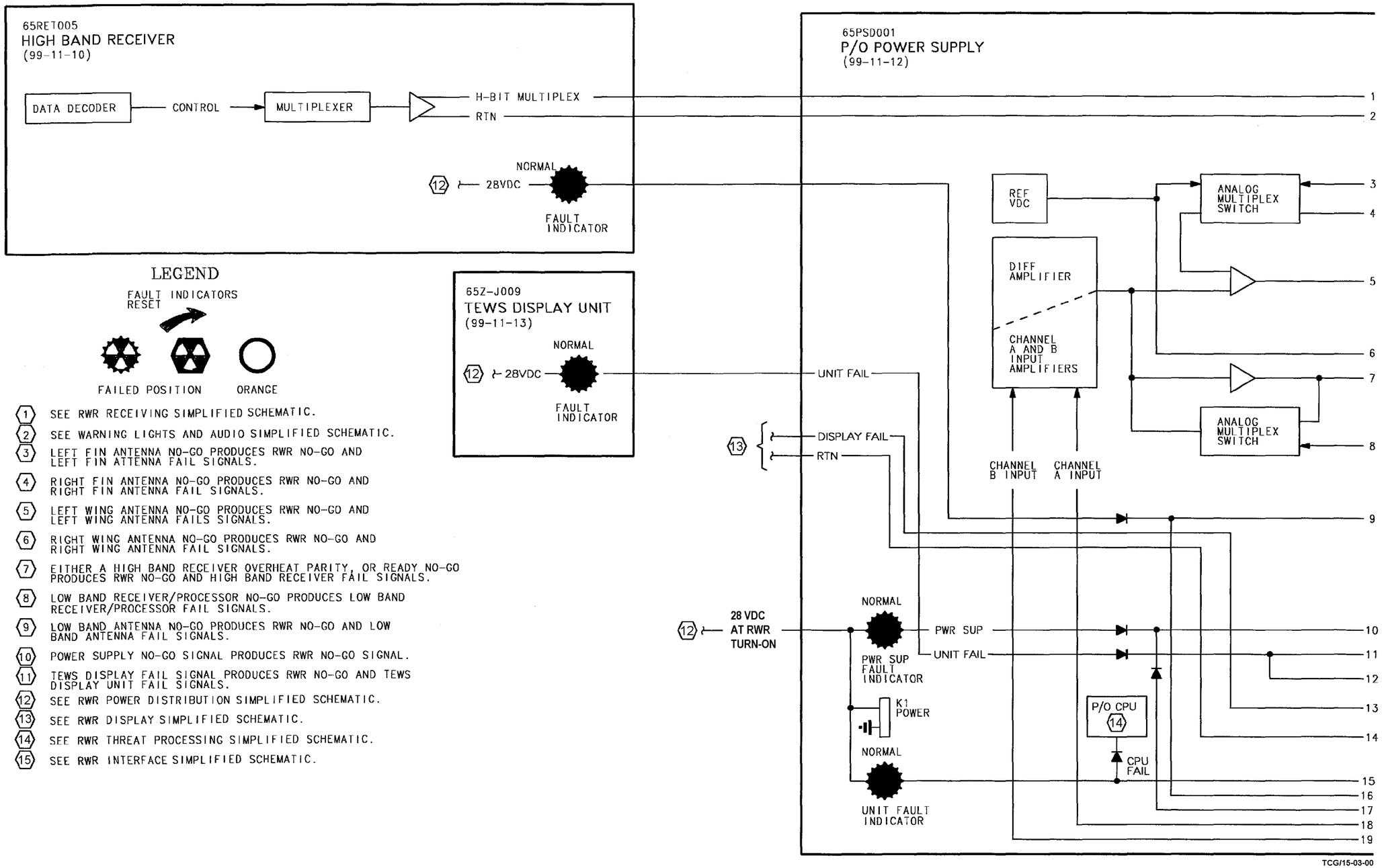
11-411. Radar Set. The RWR receives the antenna turnaround signal and radar signal reference when the radar is operating in some modes. These signals are used by the RWR with blanker information to determine whether or not there is a tracking radar threat operating in the same frequency spectrum as that of the radar.

11-412. Blanker. Low band blanking information is received from channel 7 line driver within the blanker by the low band blanking circuit. The low band blanking circuit produces a low band blanking signal depending upon TACAN frequency information derived from the CC data to the threat processing circuits. High band blanking information is received from channel 8 line driver by the high band blanking circuit. The high band blanking circuit provides a high band blanking signal to the threat processing circuits depending on radar frequency and mode information derived from the CC data and presence of the antenna turnaround signal from the radar transmitter.

1-413. CMD. The RWR requests stores inventory and program identification information from the CMD. The stores inventory will be requested and displayed within 2 seconds after the RWR receives the CMD BIT display discrete. After start of initiated BIT, the CMD will provide a discrete signal to the low band receiver/ processor indicating when stores loading information may be requested by the RWR. The discrete signal will remain set (enabled) until the RWR sends the first request for stores word. The CMD will provide the RWR with CMD program identification and stores inventory in response to an RWR request for CMD inventory.

11-414. ICMS. The RWR interfaces with set 2, set 3 and band 3 (set 1). The interface with set 2 and set 3 are identical and therefore only the set 2 will be discussed. The RWR receives reprogram requests from set 2 when immediate communicationand/or program instructions are needed. The RWR and ICMS transfer data via the data link. The data exchanged contains OFP, PFM, patch number, and threat data. SET 2 lookthru is used by the RWR to update threat tables when the Set 2 is not transmitting. The RWR sends a ICMS SET 2 status to the Set 2. Set 2 responses by sending a reply message to the RWR on the ICS/RWR data link. The RWR interfaces with ICMS band 3 (Set 1). Band 3 sends a program request to the RWR when immediate communications and/or program instructions are needed.

11-415. The RWR and ICMS exchange data via the ICS/RWR data link No. 1 and ICS data link No. 1. The RWR receives reprogram request log I/0 signals when



LEGEND

FAULT INDICATORS RESET

FAILED POSITION ORANGE

(1) SEE RWR RECEIVING SIMPLIFIED SCHEMATIC.

(2) SEE WARNING LIGHTS AND AUDIO SIMPLIFIED SCHEMATIC.

(3) LEFT FIN ANTENNA NO-GO PRODUCES RWR NO-GO AND LEFT FIN ATTENNA FAIL SIGNALS.

(4) RIGHT FIN ANTENNA NO-GO PRODUCES RWR NO-GO AND RIGHT FIN ANTENNA FAIL SIGNALS.

(5) LEFT WING ANTENNA NO-GO PRODUCES RWR NO-GO AND LEFT WING ANTENNA FAILS SIGNALS.

(6) RIGHT WING ANTENNA NO-GO PRODUCES RWR NO-GO AND RIGHT WING ANTENNA FAIL SIGNALS.

(7) EITHER A HIGH BAND RECEIVER OVERHEAT PARITY, OR READY NO-GO PRODUCES RWR NO-GO AND HIGH BAND RECEIVER FAIL SIGNALS.

(8) LOW BAND RECEIVER/PROCESSOR NO-GO PRODUCES LOW BAND RECEIVER/PROCESSOR FAIL SIGNALS.

(9) LOW BAND ANTENNA NO-GO PRODUCES RWR NO-GO AND LOW BAND ANTENNA FAIL SIGNALS.

(10) POWER SUPPLY NO-GO SIGNAL PRODUCES RWR NO-GO SIGNAL.

(11) TEWS DISPLAY FAIL SIGNAL PRODUCES RWR NO-GO AND TEWS DISPLAY UNIT FAIL SIGNALS.

(12) SEE RWR POWER DISTRIBUTION SIMPLIFIED SCHEMATIC.

(13) SEE RWR DISPLAY SIMPLIFIED SCHEMATIC.

(14) SEE RWR THREAT PROCESSING SIMPLIFIED SCHEMATIC.

(15) SEE RWR INTERFACE SIMPLIFIED SCHEMATIC.

Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 1 of 6)

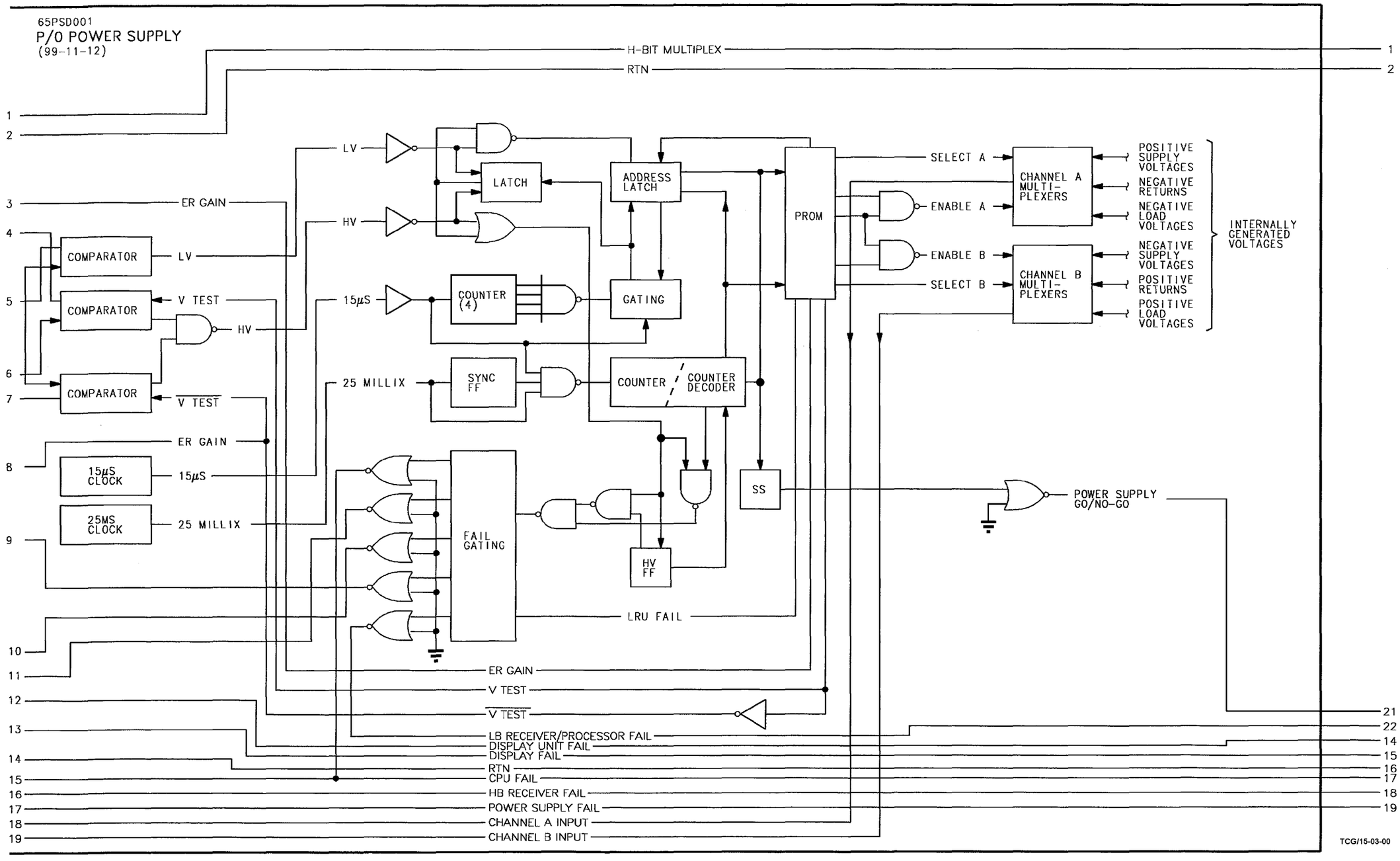


Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 2)

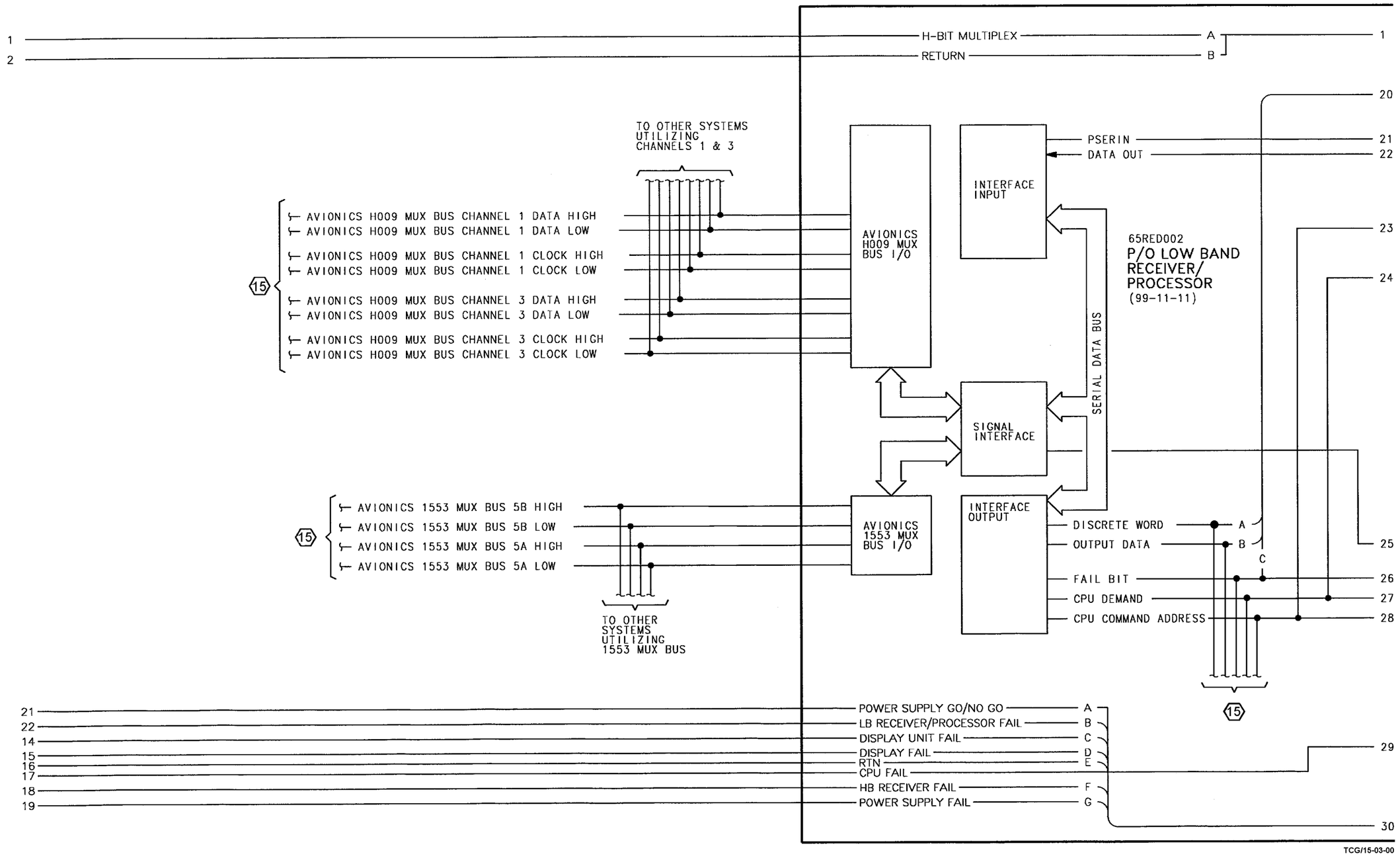


Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 3)

TO SR1F-15C-2-99GS-00-1

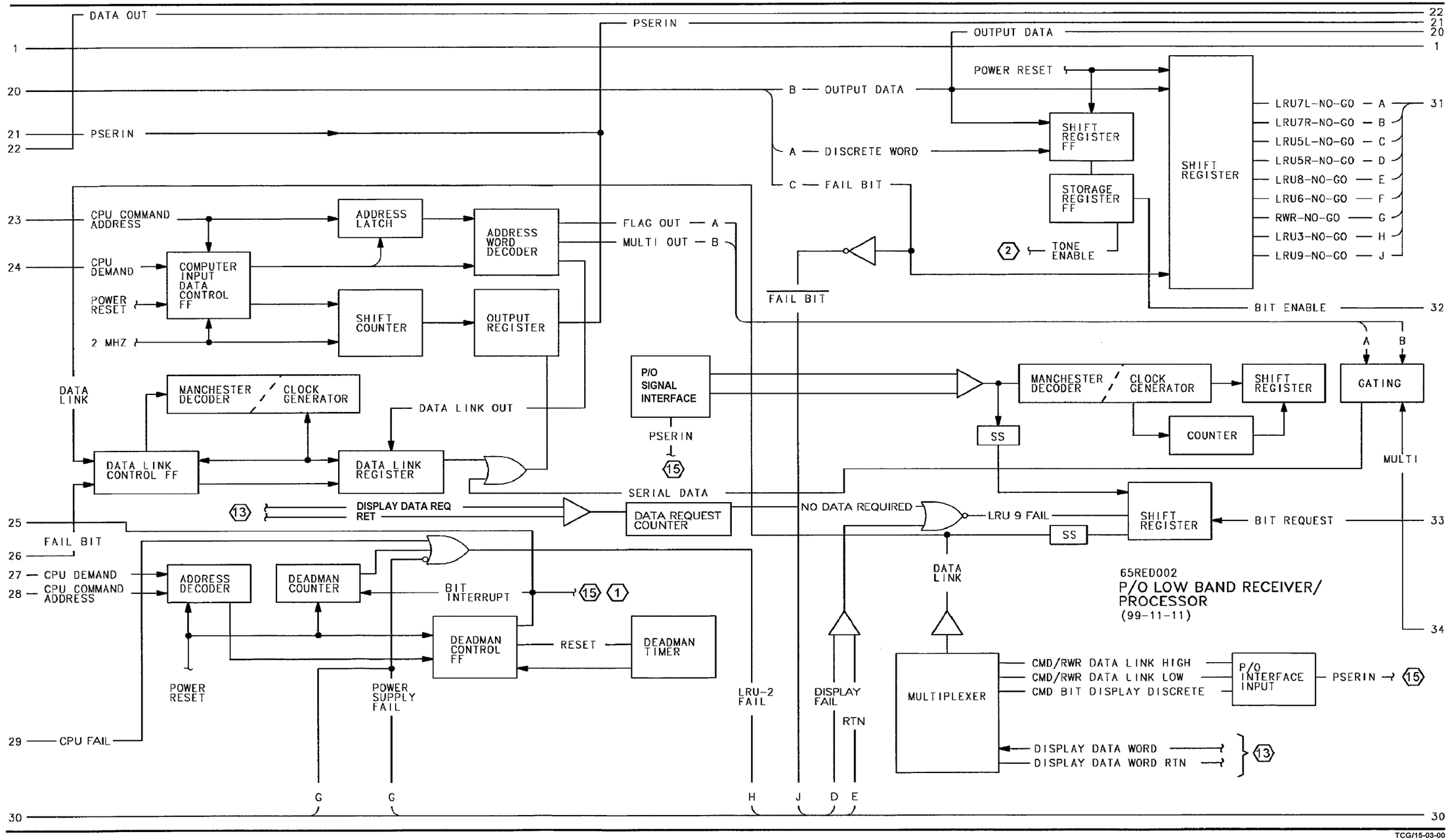


Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 4)

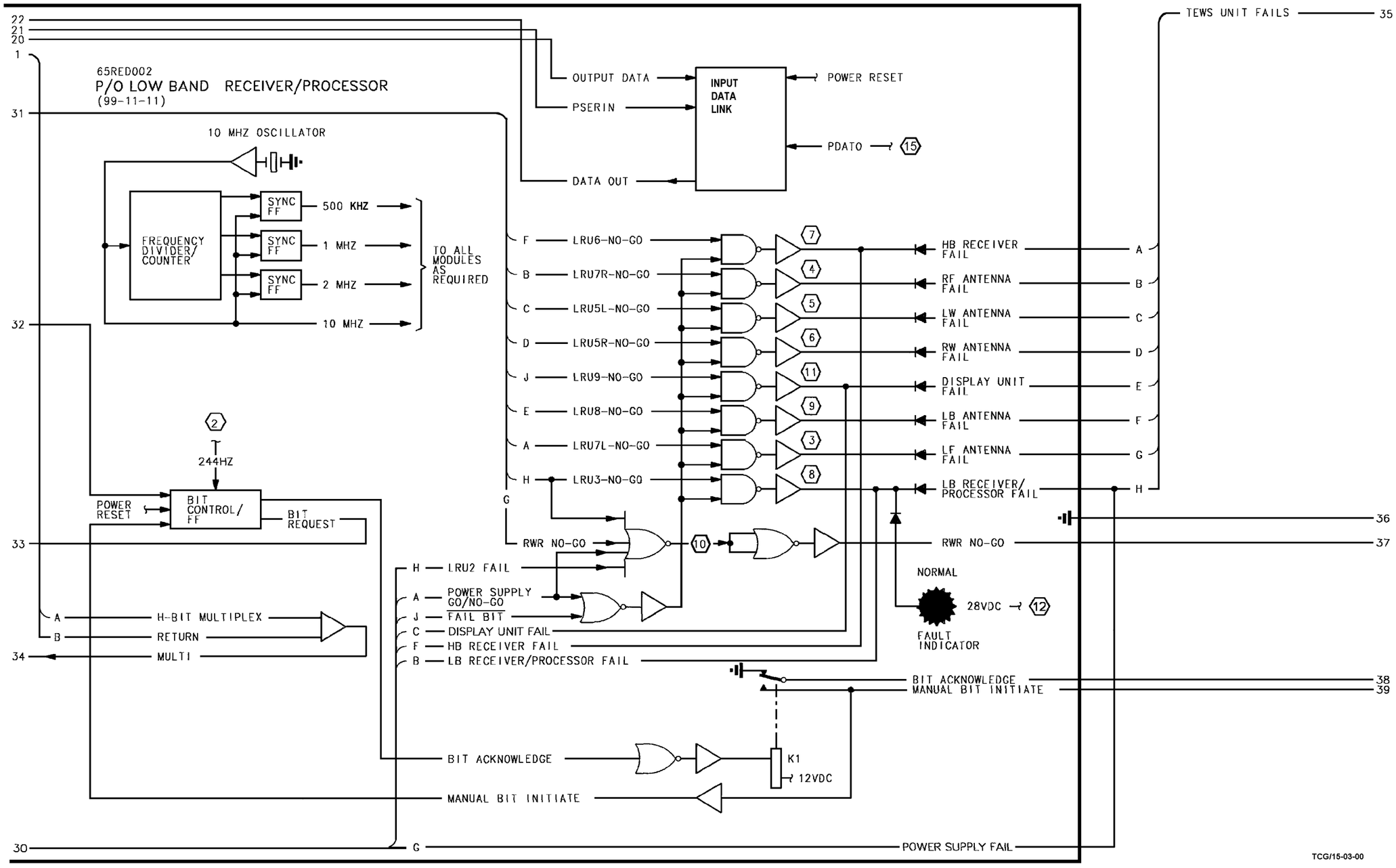


Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 5)

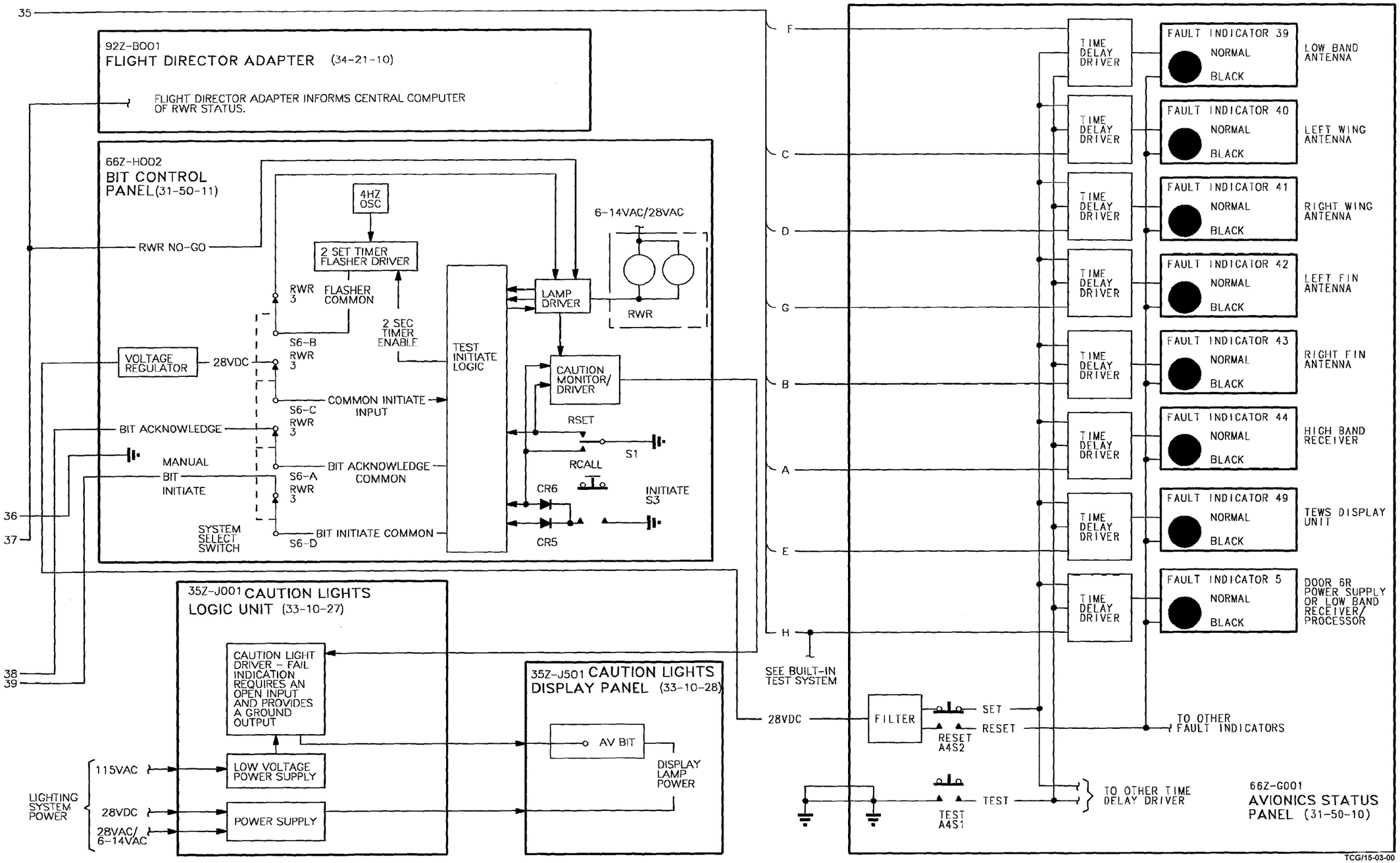
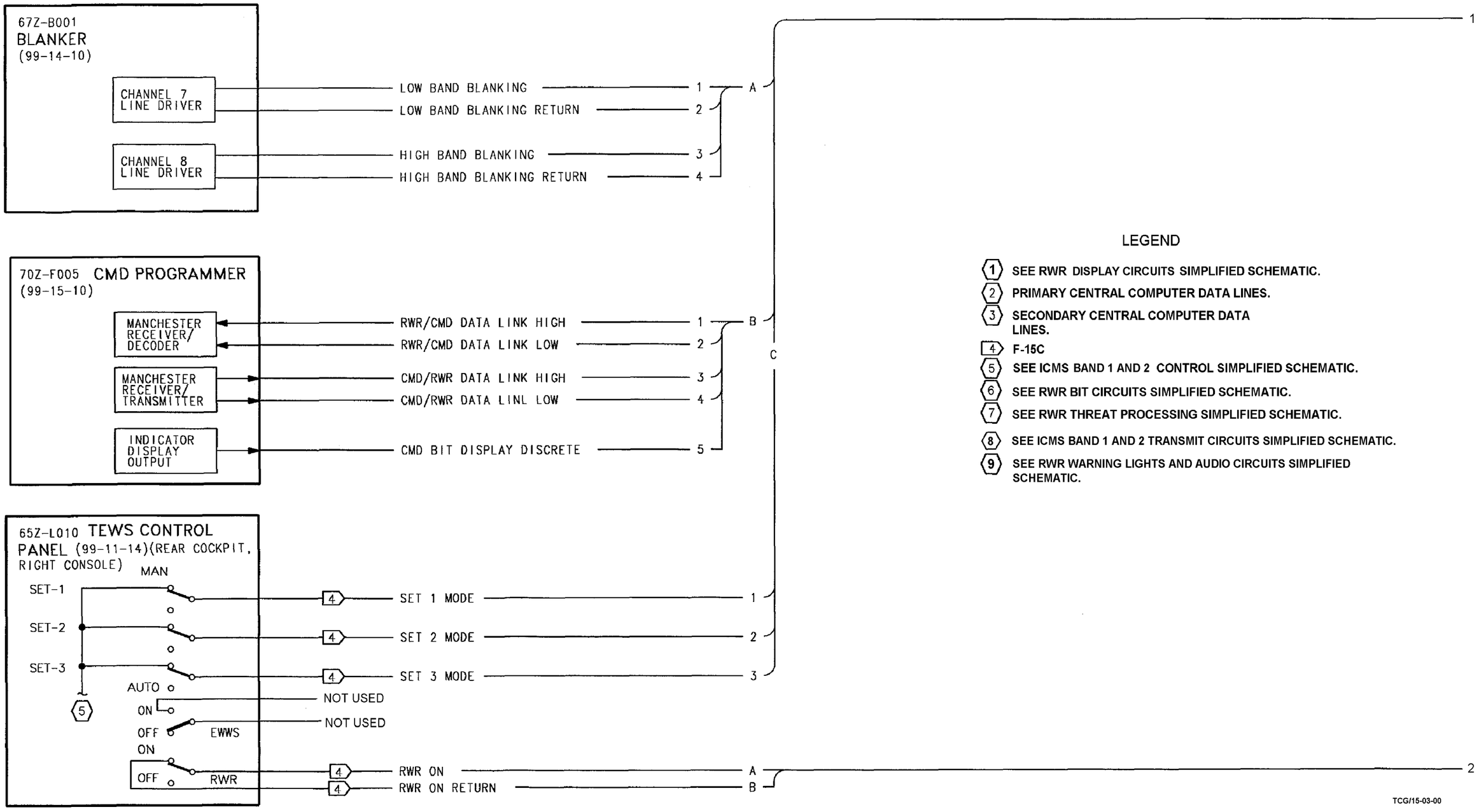


Figure 11-9. RWR BIT Circuits Simplified Schematic (Sheet 6)



LEGEND

1. SEE RWR DISPLAY CIRCUITS SIMPLIFIED SCHEMATIC.
2. PRIMARY CENTRAL COMPUTER DATA LINES.
3. SECONDARY CENTRAL COMPUTER DATA LINES.
4. F-15C
5. SEE ICMS BAND 1 AND 2 CONTROL SIMPLIFIED SCHEMATIC.
6. SEE RWR BIT CIRCUITS SIMPLIFIED SCHEMATIC.
7. SEE RWR THREAT PROCESSING SIMPLIFIED SCHEMATIC.
8. SEE ICMS BAND 1 AND 2 TRANSMIT CIRCUITS SIMPLIFIED SCHEMATIC.
9. SEE RWR WARNING LIGHTS AND AUDIO CIRCUITS SIMPLIFIED SCHEMATIC.

Figure 11-10. RWR Interface Simplified Schematic (Sheet 1 of 6)

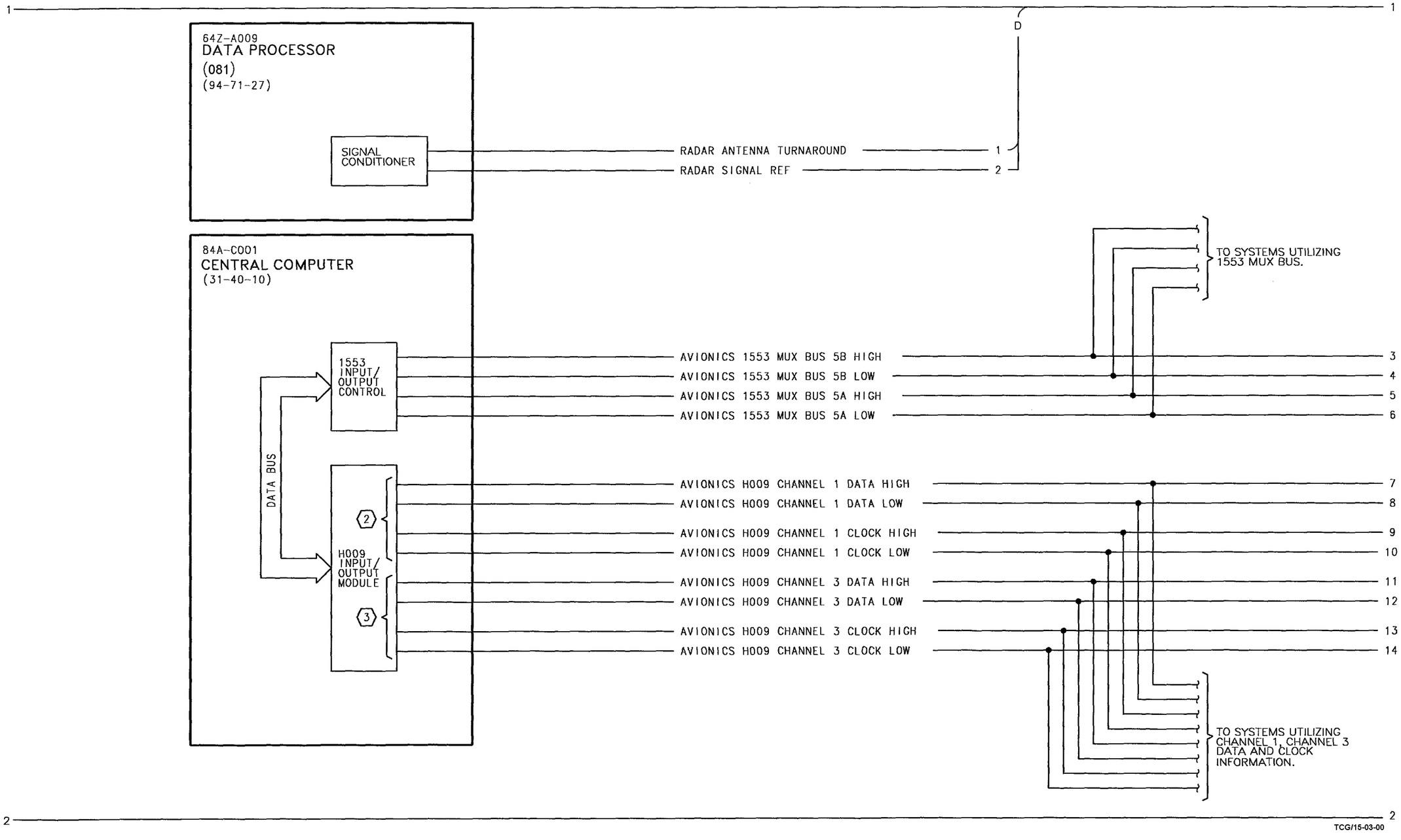


Figure 11-10. RWR Interface Simplified Schematic (Sheet 2)

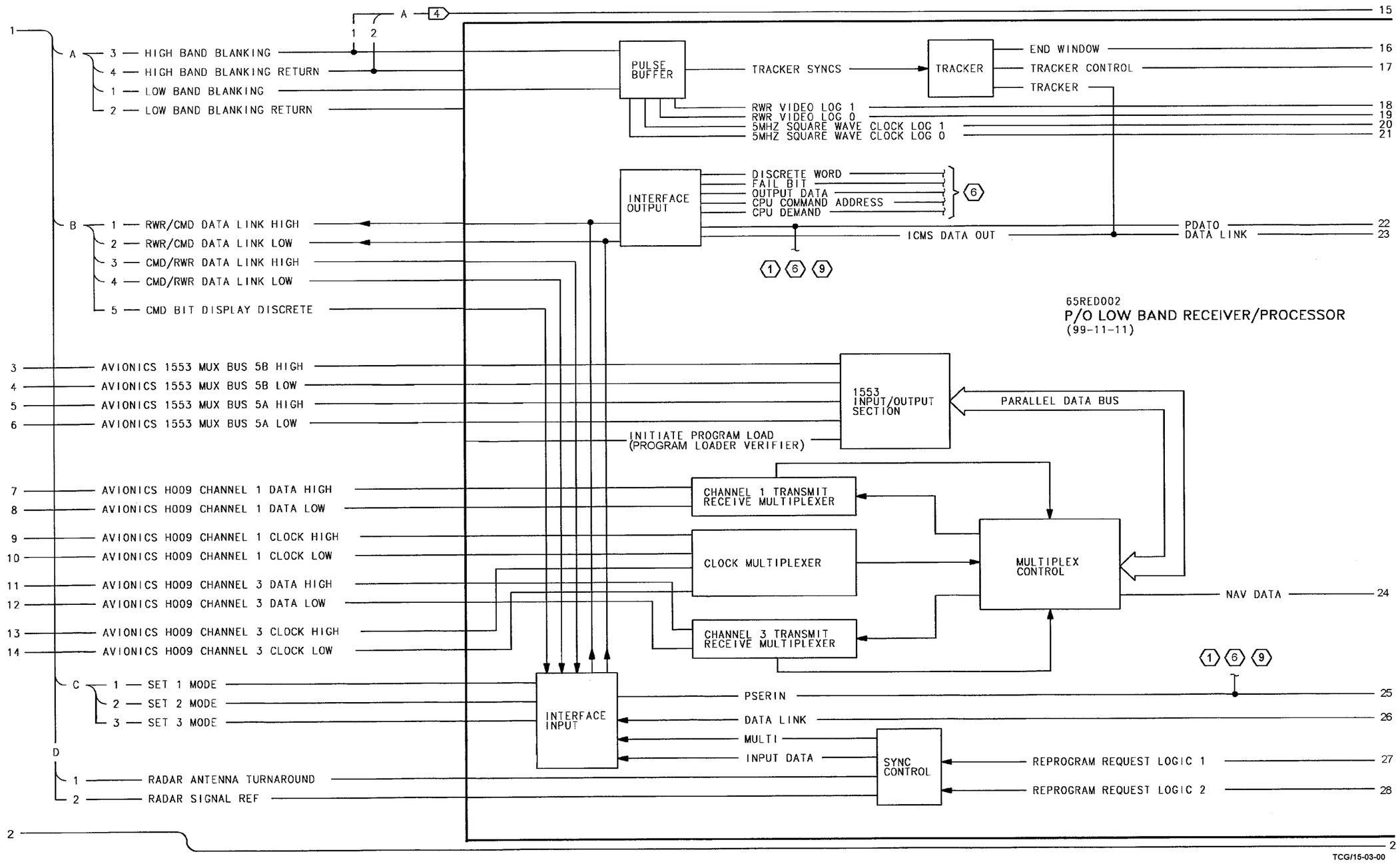


Figure 11-10. RWR Interface Simplified Schematic (Sheet 3)

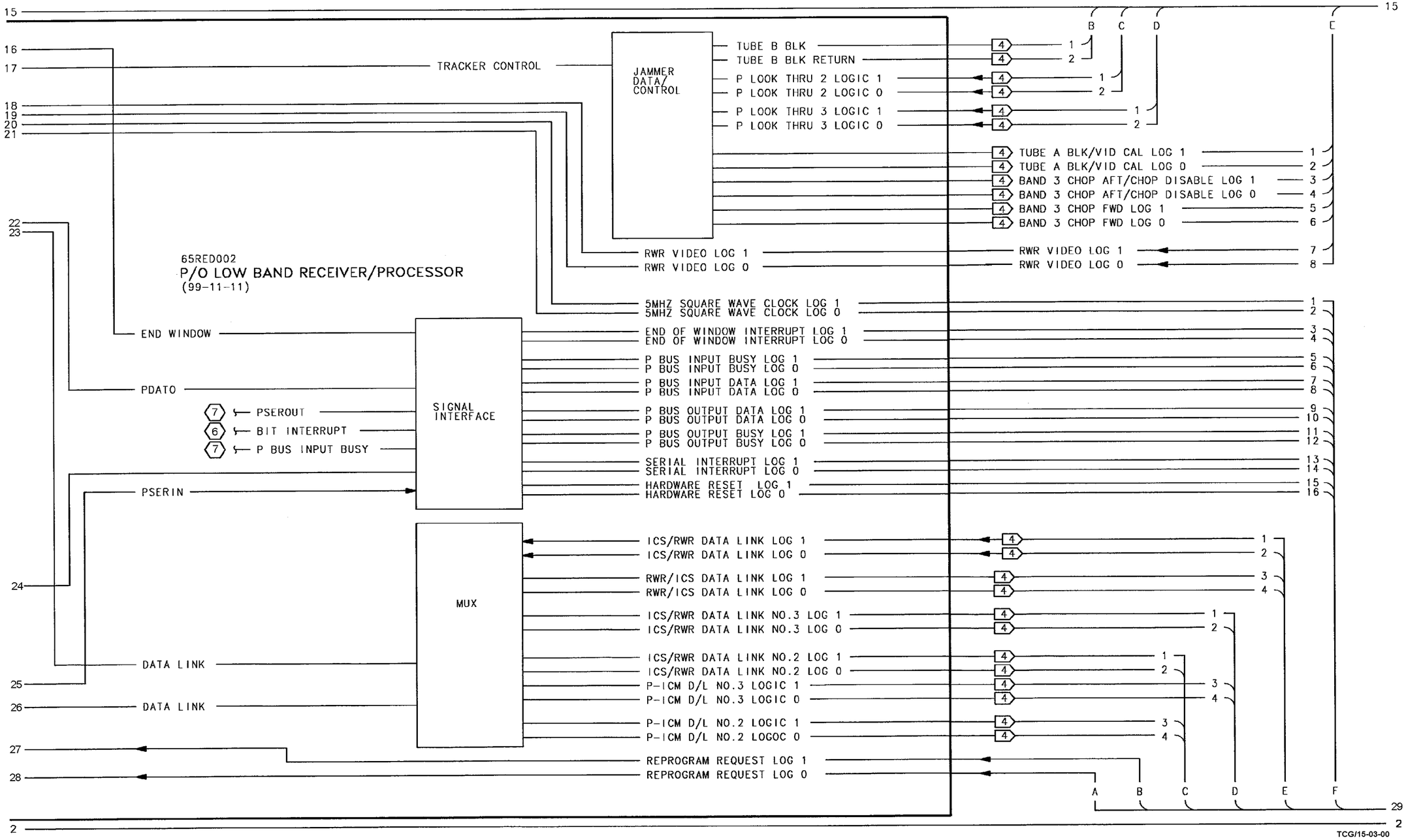


Figure 11-10. RWR Interface Simplified Schematic (Sheet 4)

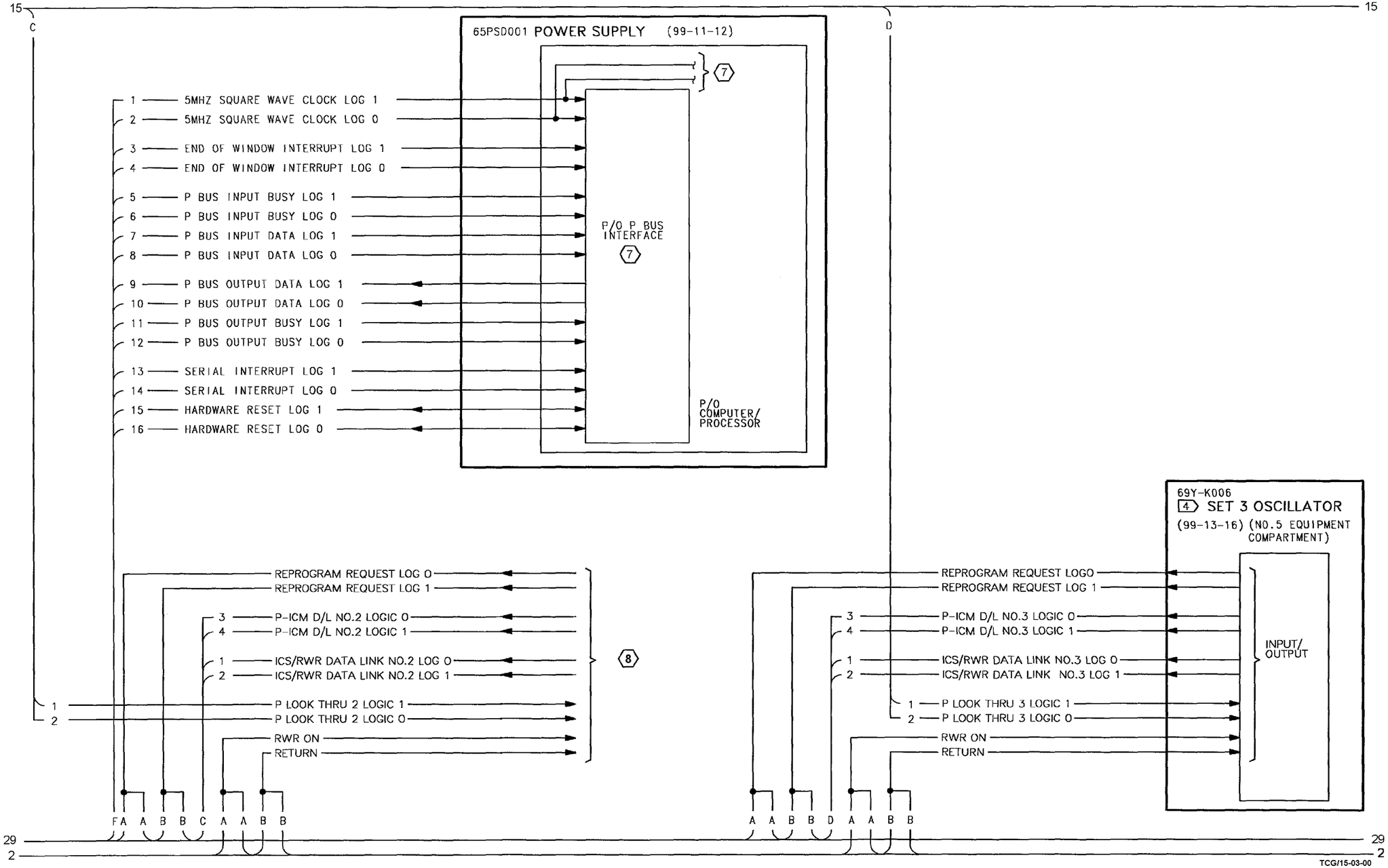


Figure 11-10. RWR Interface Simplified Schematic (Sheet 5)

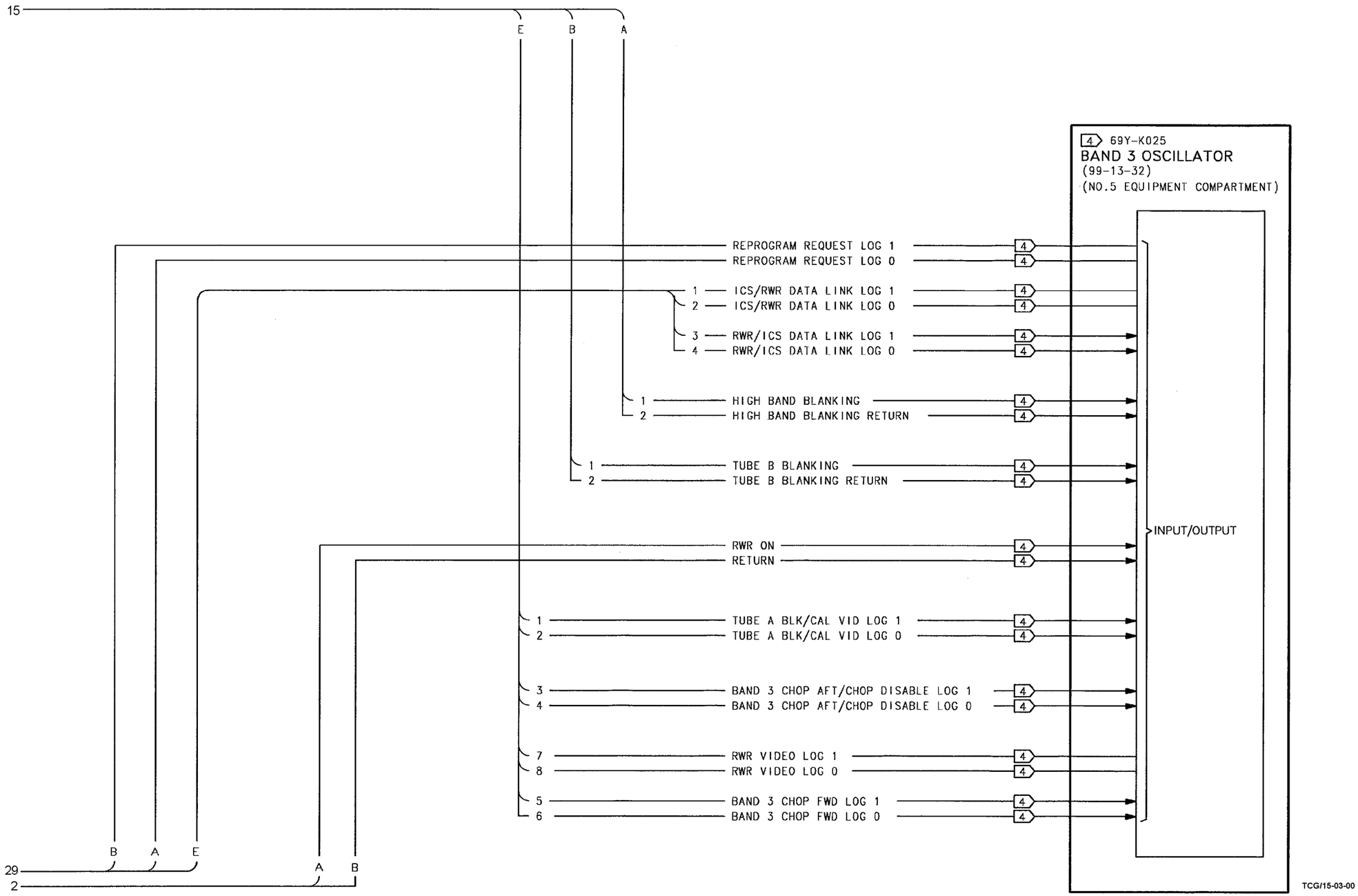


Figure 11-10. RWR Interface Simplified Schematic (Sheet 6)

the ICMS requires program instructions or immediate communication. There is a data link between the ICMS and the RWR. The data link consists of the RWRRX and the RWRTX log I/0 lines. The exchanged data contains OFP, PFM, patch number, and threat data. Additional data classified secret. Refer to TO SR1F-15C-2-99GS-00-2, Section 11.

TABLE 11-3. RWR Functional Failure Descriptions

Functional Failure	Definition
DGR LEFT FWD ANT	All signal capability degraded in this quadrant
DGR RT FWD ANT	All signal capability degraded in this quadrant
DGR LEFT AFT ANT	All signal capability degraded in this quadrant
DGR RT AFT ANT	All signal capability degraded in this quadrant
NO DF CAPABILITY	Improper DF all threats, range is correct
DF & RNG IN ERROR	Improper range and DF all threats
LETHAL RNG DGR	Loss of some threats possible. Threats displayed are correct
RNG ERROR	Improper range all threats, DF is correct
NO LOW BAND	All signal capability lost in the low band frequency
DGR LOW BAND	Loss of low band signals possible
DGR AI CAPABILITY	Loss of some ai signals possible
NO CW CAPABILITY	CW signal capability lost. Pulsed signal capability degraded
DGR CW CAPABILITY	Loss of some CW signals possible
DGR GUIDANCE	Loss of some guidance signals possible
DGR SEARCH RDR	Search radar detection capability degraded
DGR TRACK RDR	Track radar detection capability degraded
NO CMD STORES DSPL	No CMD stores information available
PRTL RWR/ICS INTG	ICMS may mask some threats
DGR RWR OPER	RWR is not reliable for any of its functions
CMD MAN MD ONLY	Auto programming of CMD unavailable
NO THRT DETECT	Failure in threat detection capabilities of the RWR. External interfaces still reliable
DGR THRT DETECT	Degradation in the threat detection capabilities of the RWR. External interfaces still operate

TABLE 11-3. RWR Functional Failure Descriptions (CONT.)

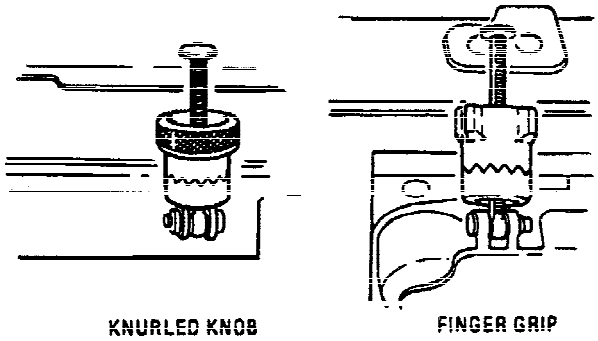
Functional Failure	Definition
MIS ID	Threats may be misidentified, DF correct
FALSE ALARMS	False threats may appear on the display
DGR RESPONSE TIME	Delayed response
MULTIPLE THREATS	Correct threat displayed as multiple threats, DF and range are correct
DGR PULSE DETECT	Pulsed signals capability degraded
DGR LFT FWD/RT AFT	All signal capability degraded in left forward and right aft quadrants
NO LEFT FWD/RT AFT	Threats may not appear in left forward and right aft quadrants
DGR RT FWD/LFT AFT	All signal capability degraded in right forward and left aft quadrants
NO RT FWD/LEFT AFT	Threats may not appear in right forward and left aft quadrants
C1 BAND DGR	[1] All signal capability degraded in the C1 frequency region
Cl BAND INOP	[1] Loss of all signals in the C1 frequency region
C2 BAND DGR	[1] All signal capability degraded in the C2 frequency region
C2 BAND INOP	[1] Loss of all signals in the C2 frequency region possible
C3 BAND DGR	[1] All signal capability degraded in the C3 frequency region
C3 BAND INOP	[1] Loss of all signals in the C3 frequency region possible
C4 BAND DGR	[1] All signal capability degraded in the C4 frequency region
C4 BAND INOP	[1] Loss of all signals in the C4 frequency region possible
C5 BAND DGR	[1] All signal capability degraded in the C5 frequency region
C5 BAND INOP	[1] Loss of all signals in the C5 frequency region
LRU-9 DISP INOP	The LRU-9 display is not operational. Threat detection and warning tone capability of the RWR is not degraded.
INCOMPAT TEWS DISP	LRU-9 is not the P31 type of display.

[1] Refer to TO SR1F-15C-2-99GS-00-2 for classified definition

11-416. **SPECIAL MAINTENANCE REQUIREMENTS.**

11-417. **FASTENERS.** Refer to applicable paragraph below.

11-418. **LRU Spring Lock Fastener Loosening and Tightening.**



Two types of LRU spring lock fasteners are used. One fastener has a knurled knob and the other a knob with four finger grips.

11-419. Loosening.

1. Pull knob out to release serrated collar and turn ccw until knob no longer engages collar when released.

CAUTION

2. Turn knob CCW until collar can be pulled up enough to rotate swivel bolt down to clear mounting foot on LRU.

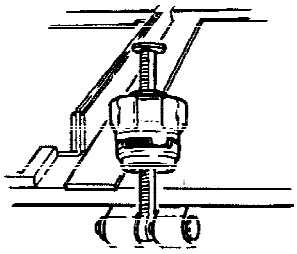
11-420. Tightening.

1. Rotate swivel bolt up until serrated collar engages mounting foot on LRU.

2. Turn knob CW until knob is tight.

3. Gently push LRU in and turn knob until tight.

11-421. **LRU Ratchet Fastener Loosening and Tightening.**



CAUTION

To prevent damage to fasteners, do not use hand tools to tighten or loosen knobs.

11-422. Loosening.

1. Turn knob CCW until swivel bolt can be rotated down to clear mounting foot on LRU.

11-423. Tightening.

1. Rotate swivel bolt to engage LRU mounting foot.

2. Turn knob CW to tighten knob.

3. Gently push LRU in and turn knob until tight.

11-424. **CONSUMABLE MATERIALS LIST.**

11-425. **SUPPLIES (CONSUMABLES).** A list of supplies required to support the organizational maintenance of the RWR system is provided in Table 11-4.

11-426. **SUPPORT EQUIPMENT LIST.**

11-427. **TEST EQUIPMENT.** Test equipment required for maintenance of the RWR system is listed in Table 11-5.

11-428. **SPECIAL TOOLS.** Special tools required for maintenance of the RWR system are listed in Table 11-6.

Table 11-4. Supplies (Consumables)

Nomenclature	Material	Part Number (CAGE)
Adhesive - sealant	Silicone	MIL-A-46146 TY1 (80244)
Cleaning compound		MMS409 (76301)
Insulation tape	Self-adhesive high temperature foil	BL15462-1 (92798)
Insulation tape	Self-adhesive foil	BL19799-75 (9798)
Lockwire	Non-electrical	MS20995NC20 (96906)
Primer		DC 1200 (71984)
Sealing compound	Silicone	PR1750Bl-2 (83574)
Tape, lacing	Nylon	MIL-T-43435TYPE-2SIZE-3FINISH-E (81349)
Tape, lacing	Nylon	MIL-T-43435,TYPE,4FNSHD,S1ZE3 (81349)
Tape, self adhesive	Teflon	MILT23594TY1-1.00 (81349)

Table 11-5. Test Equipment List

Equipment Number	Nomenclature	Use and Application
AN/PSM-37/AN/PSM-6 (alternate)	Multimeter	Trouble Analysis
AN/APM-427	Improved Radar Simulator (IRS)	Refer to 99-11-04
AN/ASM-700	Program Loader Verifier Test Set	Refer to 99-11-03, 99-11-04
H133C/AIC	Headset, Microphone	Refer to 99-11-04
5-62887-1	Cord Assembly, Electric	Refer to 99-11-04

Table 11-6. Special Tools List

Tool Number	Nomenclature	Use and Application
68D410027-1001	Pliers, Retaining Ring	Refer to 99-11-26, 99-11-29, 99-11-30, 99-11-31, 99-11-32.
68D410027-2001	Tool, Cable Puller	Refer to 99-11-26, 99-11-29, 99-11-30, 99-11-31, 9911-32.

SECTION XIII

COUNTERMEASURES SET AN/ALQ-135E/(V) (ICMS) - F-15C

13-1. SYSTEM FUNCTIONAL DESCRIPTION.

13-2. This section contains maintenance instructions for Countermeasures Set AN/ALQ-135E/(V), referred to as the ICMS, which is made up of the equipment listed in Table 13-1. The ICMS is part of the Tactical Electronic Warfare System (TEWS) used on the F-15C aircraft.

13-3. The function of the ICMS within the TEWS is to oppose surface-to-air missile, airborne interceptors, and anti-aircraft artillery attacks with active electronic countermeasures (ECM) and a minimum of pilot activity. The ICMS Band 1/Band 2/Band 3 are normally controlled by Radar Warning Receiver AN/ALR-56C (referred to as the RWR). The RWR detects and analyzes the threat environment and determines the most effective ECM that the ICMS can provide to oppose the threat environment as it exists at that instant. The RWR then sends instructions to the ICMS in the form of digital words which program the ECM parameters required for the most effective jamming modulations and frequency assignments. Under emergency conditions, the ICMS can use its internal programmers to control these parameters so that ECM coverage is provided without RWR data. The ICMS has built-in test (BIT) that monitors various operating parameters and sets BIT indicators in the event of a failure.

13-4. **DESCRIPTION.** See Figures 13-1 and 13-3. The ICMS is made up of three independent countermeasures sets of which two sets (Band 1 and 2) are made up of an Oscillator, RF Amplifier, and Antenna. The other set is Band 3 which is made up of an Oscillator, Preamplifier, two RF Amplifiers (FWD and Aft) each with a related Pulse and CW antenna providing forward and aft coverage. The Band 1 set operates in the E through G bands, Band 2 set operates in the G and H band and the Band 3 operates in the H, I and J band.

13-5. During operation in the auto (normal) mode, an ICMS control word, from the RWR, is used to select jamming mode, establish jamming priorities and determine the jamming frequency(ies) to be covered. Operation is under the total control of the RWR. During manual (emergency) operation, all jamming parameters are controlled by data words stored in the self-contained programmer. For classified description refer to TO SR1F-15C-2-99GS-00-2.

13-6. **LINE REPLACEABLE UNITS.** ICMS system line replaceable units (LRU) are identified and listed in Table 13-1. System configuration is designed for maximum flexibility; however, the standard set configuration is listed in Table 13-2.

13-7. **COMPONENT DESCRIPTION.** The paragraphs below describe the ICMS Band 1/Band 2/Band 3 (Set 3, Set 2, and Set 1) units. Each unit is hard mounted and, where required, cooled by the aircraft environmental control system (ECS) which provides the required air flow and cooling capacity to dissipate heat.

13-8. **Set 3 Antenna (99-13-12).** Set 3 antenna (Band 1) is a coaxial cable fed, omnidirectional, broad band, blade type antenna.

13-9. **Set 2 Antenna (99-13-14).** Set 2 antenna (Band 2) is a waveguide fed, broad band, omnidirectional, blade type antenna.

13-10. **Set 1 Fwd Up Antenna (99-13-35).** Set 1 (Band 3) FWD up antenna is a coaxial cable fed horn, pulse/CW antenna. Together with the Band 3 FWD down antenna they provide a cone of coverage forward of the aircraft.

13-11. **Set 1 Fwd Down Antenna (99-13-36).** Set 1 (Band 3) FWD down antenna is a waveguide fed, horn, pulse/CW antenna. Together with the Band 3 FWD up antenna they provide a cone of coverage forward of the aircraft.

13-12. **Set 1 Aft Antenna (99-13-37).** Set 1 (Band 3) upper element is a coaxial cable fed horn, CW antenna. The lower element is a coaxial cable fed horn, pulse antenna. Each provides a cone of coverage directly aft of the aircraft.

13-13. **Set 3 Oscillator (99-13-16).** Set 3 Oscillator (Band 1) receives jamming parameter commands from the RWR and converts the commands and parameters to a low level amplitude and/or frequency modulated RF signal. In manual (emergency) mode, the jamming commands and parameters are received from a self-contained read only memory contained in the

programmer. The low level RF signal is sent to Set 3 RF Amplifier. When Set 3 Oscillator is not installed, 68R870053 ballast is installed.

13-14. **Set 2 Oscillator (99-13-16).** Set 2 Oscillator (Band 2) receives jamming parameter commands from the RWR and converts the commands and parameters to a low level, amplitude and/or frequency modulated RF signal. In manual (emergency) mode, the jamming parameters and commands are received from a self-contained read only memory contained in the programmer. The low level RF signal is sent to Set 2 RF Amplifier. When Set 2 Oscillator is not installed, 68R870053 ballast is installed.

13-15. **Band 3 Oscillator (99-13-32).** Set 1 (Band 3) Oscillator receives threat information, with or without, RWR threat information comparison which results in prioritization and jamming method selection. Tuning commands, amplitude and/or frequency modulated RF, and frequency information is sent to the Band 3 RF amplifiers. When Set 1 Oscillator is not installed, 68R870053 ballast is installed.

13-16. **Set 3 RF Amplifier (99-13-17).** Set 3 RF Amplifier (Band 1) receives the low level RF signal from the Set 3 Oscillator, amplifies and level controls the amplified RF and transmits the high level signal to Set 3 antenna through a coax cable assembly. Oscillator produced modulation is also sent to the RF Amplifier to control automatic leveling. When Set 3 RF Amplifier is not installed, 68R870053 ballast is installed.

13-17. **Set 2 RF Amplifier (99-13-18).** Set 2 RF Amplifier (Band 2) receives the low level RF signal from the oscillator, amplifies and level controls the RF signals and transmits the high level signal to Set 2 antenna through waveguide transmission lines. Oscillator produced modulation is also sent to the RF Amplifier to control automatic leveling. When Set 2 RF Amplifier is not installed, 68R870053 ballast is installed.

13-18. **Band 3 RF Amplifiers (Fwd and Aft) (99-13-31 and 99-13-33).** Band 3 (Set 1) RF Amplifiers provide jamming program initiation CW or pulse selection, tuning and final TWT amplification. The RF signals from the Band 3 RF Amplifier (Aft) use cable assemblies for application to the Band 3 aft antenna. The RF signals from the Band 3 RF Amplifier (FWD) use waveguide for application to the Band 3 FWD up and down antennas. When Set 2 RF Amplifier is not installed, 68R870053 ballast is installed.

13-19. **Band 3 Preamplifier (99-13-34).** The Band 3 Preamplifier provides initial system amplification of received RF threat signals or BIT RF signals. The RF signals are selected, amplified, and sent to the Band 3 Oscillator for threat processing. Also, during BIT, the b3 bit rf signal from the Aft Band 3 RF Amplifier is used to provide a calibrated amplitude source for the Automatic Leveling Circuit (ALC).

13-20. **Programmer (99-13-19).** The programmer is a small matrix device which provides Band 1 and Band 2 Oscillators with predetermined program inputs. The predetermined program inputs are used by the ICMS when operating in manual mode. A separate programmer is provided for each oscillator installed in the aircraft.

13-21. **Summing Network (99-13-20).** The summing network receives RF samples from the RF amplifiers and applies a composite output of these samples to the RWR high band receiver.

13-22. **Cable Assembly (99-13-22 and 23).** A coaxial cable assembly with special low loss characteristics is used to couple the RF Amplifier output from Band 1 and 2 to the respective antenna. The cable assembly is installed in the aircraft in a way which allows stowage when not in use.

13-23. **Cable Assembly (99-13-53 THRU 99-13-57).** Two sets of low loss coaxial cables, CW and pulse - FWD and CW and pulse - aft, are used as an RF path from the Band 3 RF Amplifier (Aft) to the Band 3 aft tail cone antenna. Cable assembly (FWD up) is used to couple the waveguide (FWD up) to the Band 3 FWD up antenna.

13-24. **Waveguide (99-13-24 THRU 99-13-30).** A pressurized waveguide couples the output of Band 2 RF Amplifier to Band 2 antenna. The Set 2 (center) requires three sections of waveguide and the Set 3 (Aft) requires two sections of waveguide. When a Band 2 configuration is not used, the waveguides are secured to the aircraft structure in a stowed position. When waveguides are unused and stowed, pressurization integrity is preserved by quick-disconnect end caps.

13-25. **Waveguide (99-13-38 THRU 99-13-40).** Two sections of pressurized waveguide couple the CW and pulse outputs for the Band 3 RF Amplifier (FWD) to a magic tee. The forward up combined output is coupled thru six sections of waveguide to a coax adapter. The

forward down combined output is coupled thru four waveguide sections.

13-26. **Coax Adapter (99-13-48, 58, and 59).** The coax adapters are used to couple RF from waveguide port to the cable assembly.

13-27. **Magic Tee (99-13-41).** The magic tee is used to couple Band 3 CW and pulse RF to the forward up and forward down waveguide sections.

13-28. **Related Component Description.** The paragraphs below give a description of components related to the ICMS system.

13-29. TEWS Control Panel. The TEWS control panel, a component of the RWR, contains the ICS ON/OFF switch, SET-1 switch, SET-2 switch, SET-3 switch, SET-1 FAIL light, SET-2 FAIL light, and SET-3 FAIL light.

13-30. TEWS IA Control Panel. The TEWS IA control panel, a component of RWR, contains the ICS MAN/ AUTO/STBY switch, and the RWR/ICS, COMBAT/ TRNG switch.

Table 13-1. Line Replaceable Units

Common Name	S/S/SN	Ref. Des.	Nomenclature
Programmer, Set 2 and Set 3	99-13-19		Programmer, Electronic Command Signal MX-9412(V)/ALQ-135(V)
Summing Network	99-13-20	69E-K010	Network Summation CU-2081/ALQ-135(V)
Cable Assembly	99-13-22	69W-K509	Cable Assembly
Cable Assembly	99-13-23	69W-K510	Cable Assembly
Cable Assembly	99-13-53	69W-A527	Cable Assembly
Cable Assembly	99-13-54	69W-T528	Cable Assembly
Cable Assembly	99-13-55	69W-T529	Cable Assembly
Cable Assembly	99-13-56	69W-T530	Cable Assembly
Cable Assembly	99-13-57	69W-T531	Cable Assembly
Set 2 Antenna (Band 2)	99-13-14	69E-D008	Antenna, AS-2903/ALQ-135(V)
Set 2 RF Amplifier or 1 ▶ 68R870053 Ballast	99-13-18	69ARK002	Amplifier, Radio Frequency AM-6598/ALQ-135(V)
Set 2 and 3 Oscillator or 1 ▶ 68R 870053 Ballast	99-13-16	69Y-K006 69Y-K005	Control-Oscillator C-9341(P)/ALQ-135(V) or Control-Oscillator C-9342(P)/ALQ-135(V)
Set 3 Antenna (Band 1)	99-12-12	69Y-K004	
Set 3 RF Amplifier or 1 ▶ 68R870053 Ballast	99-13-17	69ARK003	Amplifier, Radio Frequency AM-6597/ALQ-135/(V)
Band 3 Aft Antenna (Set 1)	99-13-37	69E-T033	Antenna, AS-3989/ALQ-135C(V)
Band 3 FWD Down Antenna	99-13-36	69E-B037	Antenna, AS-3816/ALQ-135B(V)

Table 13-1. Line Replaceable Units (CONT.)

Common Name	S/S/SN	Ref. Des.	Nomenclature
Band 3 FWD Up Antenna	99-13-35	69E-B031	Antenna, AS-3817/ALQ-135C(V)
Band 3 Oscillator or 1 ▶ 68R870053 Ballast	99-13-32	69Y-K025	Control Oscillator, C-12023/ALQ-135C(V)
Band 3 RF Amplifier (Aft)	99-13-33	69ART030	Amplifier, Radio Frequency, AM-7397/ ALQ-135C(V)
Band 3 RF Amplifier (FWD) or 1 ▶ 68R870053 Ballast	99-13-31	69ARK024	Amplifier, Radio Frequency, AM-7397/ALQ-135C(V)
Band 3 Preamplifier	99-13-34	69ART034	Amplifier, Radio Frequency, AM-7311A/ALQ-135C(V)
Magic Tee	99-13-41	69W-K519	Not Assigned
Coax Adapter	99-13-48	69W-A526	Not Assigned
Coax Adapter	99-13-58	69W-T532	Waveguide/Coaxial Adapter
Coax Adapter	99-13-59	69W-T533	Waveguide/Coaxial Adapter
Waveguide	99-13-24	69W-D514	Waveguide Assembly
Waveguide	99-13-25	69W-K506	Waveguide Assembly
Waveguide	99-13-26	69W-N507	Waveguide Assembly
Waveguide	99-13-27	69W-G513	Waveguide Assembly
Waveguide	99-13-30	69W-D516	Waveguide Assembly
Waveguide	99-13-38	69W-B504	Waveguide Assembly
Waveguide	99-13-39	69W-K517	Waveguide
Waveguide	99-13-40	69W-K518	Waveguide
Waveguide	99-13-42	69W-K520	Waveguide
Waveguide	99-13-43	69W-K521	Waveguide
Waveguide	99-13-44	69W-K522	Waveguide
Waveguide	99-13-45	69W-K523	Waveguide
Waveguide	99-13-46	69W-A524	Waveguide
Waveguide	99-13-47	69W-A525	Waveguide

Table 13-1. Line Replaceable Units (CONT.)

Common Name	S/S/SN	Ref. Des.	Nomenclature
Waveguide	99-13-49	69W-G511	Waveguide
Waveguide	99-13-50	69W-D515	Waveguide
Waveguide	99-13-51	69W-D512	Waveguide
Waveguide	99-13-52	69W-B503	Waveguide
1 ▶ 68R870053 ballast is installed when appropriate RF Amplifier/Oscillator is not installed.			

Table 13-2. Configuration Table

BAND	COMPONENTS	BAND	COMPONENTS	BAND	COMPONENTS
3	Fwd Up Antenna AS-3816/ALQ-135B(V); Fwd Down Antenna AS-3817/ ALQ-135B(V); Aft Antenna AS-3989/ ALQ-135C(V)	2	Antenna AS-2903/ ALQ-135/(V)	1	Antenna AS-2902/ ALQ-135/(V)
	Oscillator C-12134/ ALQ-135(V)		Oscillator C-9342(P)/ ALQ-135/(V)		Oscillator C-9341(P)/ ALQ-135/(V)
	RF Amplifier (FWD) RF Amplifier (Aft) AM-7397/ ALQ-135C(V)		RF Amplifier AM-6598/ ALQ-135/(V)		RF Amplifier AM-6597/ ALQ-135/(V)
	Preamplifier AM-7311A/ ALQ-135C(V)		Programmer MX-9412(V)/ALQ-135(V). Refer to TO SR1F-15C-8-1		Programmer MX-9412(V)/ALQ-135(V). Refer to TO SR1F-15C-8-1

13-31. **List of Mnemonics/Signal Names.** This is a list of mnemonics/signal names used throughout this section and their definitions.

Name	Definition
NOTE An asterisk beside a signal name indicates the signal is active low.	
a ant l	Aft antenna left
a ant r	Aft antenna right
abiscv	Channel A video/ isolation calibration video
afwpwrl	Channel A forward

Name	Definition
	power low
ahtoi	Channel A TWT modulator heater overcurrent
ahtui	Channel A TWT modulator heater undercurrent
ahvry	Channel A high voltage ready
alc	Automatic leveling control
alcon	Automatic leveling control on
amobk	Channel A TWT modulator blank
amoecl	TWT modulator U1 emitter coupled logic
amoot*	Channel A TWT modulator overtemperature
ampbit*	Amplifier built-in test
atten rf-a and -b	Channels A and B attenuation RF
atucoalc	Agile tuning unit control oscillator automatic leveling control
atu0, atul	Agile tuning unit 0 and agile tuning unit 1
atu(0,1)am(0,1)	Agile tuning unit (atu0 and atul) amplitude modulation bits 0 and 1
atu(0,1)fc	Agile tuning unit (atu0 and atul) fast clock
atu(0,1)fd	Agile tuning unit (atu0 and atul) fast data
atu(0,1)on*	Agile tuning unit (atu0 and atu1) on
atu(0,1)ps(0-5)	Agile tuning unit (atu0 and atu1) program select bits 0 through 5
atu(0,1)rfasel*	Agile tuning unit (atu0 and atul) RF Amplifier select
atwot	Channel A TWT over temperature
avionics 1553 mux bus 5(A,B)	1553 direct coupled data
bblk	Channel B blank
bfwpwrl	Channel B forward power low
bhtoi	Channel B TWT modulator heater overcurrent
bhtui	Channel B TWT modulator heater undercurrent
bhvry	Channel B high voltage ready
bitack	Built-in test acknowledged
bit/clt	Built-in test/closed loop tuning
bittest	Built-in test testing
bmobk	Channel B TWT modulator blank
bmoot*	Channel B TWT modulator overtemperature
btwot	Channel B TWT over temperature
b3 bit rf	Band 3 built-in test RF
b3blkrq*	Band 3 blank request
b3chopmd*	Band 3 chop mode
b3clt/rcv*	Band 3 closed loop

Name	Definition
	tuning/receive
b3(f/a)rf	Band 3 forward or aft RF
b3forjclk	Band 3 forward chop clock
b3fuop*	Band 3 full operate
b3lvpstherdn*	Band 3 low voltage power supply temporarily down
b3scpubit	Band 3 system control processor unit built-in test
b3rcvr rf	Band 3 receiver RF
b3rf	Band 3 RF
b3rfs/h	Band 3 sample and hold
b3rrj clk	Band 3 aft chop clock
b3r0rst	Band 3 (forward) RF Amplifier reset
b3r(0,1)ae*	Band 3 (forward and aft) RF Amplifier channel A TWT modulator enable
b3r(0,1)be*	Band 3 (forward and aft) RF Amplifier channel B TWT modulator enable
b3r(0,1)cb	Band 3 (forward and aft) RF Amplifier command bus
b3r(0,1)cmdack*	Band 3 (forward and aft) RF Amplifier command acknowledged
b3r(0,1)fltflg	Band 3 (forward and aft) RF Amplifier fault flag
b3r(0,1)ft*	Band 3 (forward and aft) RF Amplifier fault
b3r(0,1)pten	Band 3 (forward and aft) RF Amplifier power test enable
b3r(0,1)rb	Band 3 (forward and aft) RF Amplifier reply bus
b3r(0,1)tempdn*	Band 3 (forward and aft) RF Amplifier temporarily down
b3r(0,1)wucmpl*	Band 3 (forward and aft) RF Amplifier warm-up complete
b3rlicson*	Band 3 aft RF Amplifier on
b3setcoft*	Band 3 set control oscillator fault
cltrf	Closed loop tuning RF
copsft*	Control oscillator power supply fault
dco(0-2)	Digitally controlled oscillator bits 0 through 2
detinh(0,1)*	Detector inhibit (rtu0 and rtul)
extablk*	External channel A blank
extbblk*	External channel B blank
extbchop*	External channel B chop
extest	External test
extlkastb*	External look through strobe
extlka*(0-3)	External look through bits 0 through 3
fantl	Forward antenna left
fantr	Forward antenna right

Name	Definition
fltord	Fault override
fsf(0-13)	Frequency screen frequency bits 0 through 13
fwdlogvid	Forward log video
fwdpwr	Forward power
gndopinh*	Ground operation inhibit
hclk(1,3)	H009 clocks 1 and 3
hdata(1,3)	H009 data 1 and 3
hilntr*	High line transient
hvlvry*	High voltage low voltage ready
hvlvsk*	High voltage low voltage synchronization
hvopgo*	High voltage operate go
hvpsft	High voltage power supply fault
hvpsot*	High voltage power supply overtemperature
hvwucz*	High voltage warm-up complete
icsauto	ICS automatic
icsmxrd*	ICS multiplex ready
icsng	ICS no-go
icson*	Band 3 forward RF amplifier on
iscv*	Isolation calibration video
indetst	Input detector strobe
inpwrl	Input power low

Name	Definition
iohven*	Input and output high voltage enable
jamstb*	Jam strobe
jamwd(0-3)	Jam word bits 0 through 3
lamptst	Lamp test
larcv*	Left aft receive
lasel*	Left aft select
lfrcv*	Left forward receive
Name	Definition
lfsel*	Left forward select
lver	Low voltage regulation
lvpsry	Low voltage power supply ready
lvsd*	Low voltage shutdown
mnlmode	Manual mode
moacn*	Channel A TWT modulator control
pcopgo*	Processor operate go
posid	Position identification
preabitd*	Preamplifier built-in test
rarcv*	Right aft receiver
rasel*	Right aft select
rfdaon*	RF distribution aft on
rfdfon*	RF distribution forward on
rfdphsh*	RF distribution phase shift
rfrcv*	Right forward receive

Name	Definition
rfsel*	Right forward select
rprq	Reprogram request
r(0-3)vid	Band 3 video
rtu0, rtu1	Repeater tuning unit 0 and repeater tuning unit 1
rtu(0,1)on*	Repeater tuning unit (RTU0 and RTU1)
rtu(0,1)rfasel*	Repeater tuning unit (RTU0 and RTU1) RF Amplifier select
rsvlogvid	Reverse log video
rvspwr	Reverse power
rwrrx	Radar warning receiver receive
rwrtx	Radar warning receiver transmit
rwrvid*	Radar warning receiver video
r(3-8)pl*	Receiver activity detector number 3 through number 8 video
scpu bus	System control processor unit bus
set1ng	Band 3 set 1 no-go
tupmd*	Time correlation unit update mode
tup(0-7)*	Time correlation unit (TCU) through TCU7) update pulse
t(0-7)atureq*	Time correlation unit (TCU0 through TCU7) agile tuning unit request
t(0-7)rcvgnt*	Time correlation unit (TCU0 through TCU7) receiver grant
vbrsense	Bridge voltage regulation sense
vps/h*	Video processor sample and hold
vswrbit*	Voltage standing wave ratio built-in test
+28vdcstby	28VDC standby voltage
40kHzdr	40 kHz drive

13-32. **PRINCIPLES OF OPERATION.** The ICMS principles of operation are shown as a description of operating controls and indicators and operation of the system functions as listed:

a. Power Distribution

b. Control Circuits

c. Transmitting Circuits

d. BIT Circuits

e. System Interface

13-33. **Controls and Indicators.** All controls and indicators used in ICMS operation are shown in Figure 13-1 and described in Table 13-3.

13-34. During flight or ground maintenance with Weight-Off-Wheels (WOW) switch enabled, current status of the ICMS is displayed on the MPCD in two different displays, the PACS Air to Air (A/A) and the tactical situation display. The status will be displayed in the lower right corner of the tactical situation display (see Figure 13-2 detail A) and the upper left corner of the PACS A/A display (see Figure 13-2 detail B). On the tactical situation display there is one line of data that represents the ICMS status. The line has three separate symbols, one for each Band. B1 represents Band 1, B2 represents Band 2 and B3 represents Band 3. Each symbol is displayed in one of three colors to indicate the status. Green indicates the band is operating without any faults. Amber indicates the band

is degraded but is still operating. Magenta indicates the band is not operational.

13-35. On the PACS A/A display the status of the ICMS is displayed in three lines of data, each line represents one band of the ICMS (see Figure 13-2 detail B). The upper line of data represents the Band 3 status. It contains three fields of data. The first field identifies the Band 3 as B3. The second field identifies the status of the Band 3 (refer to Table 13-2). The third field will only be displayed when the second field contains TMP or DGR and is used to further identify the cause of the malfunction (refer to Table 13-6). The second and third lines each only contain two fields. The first field identifies the band as B1 (Band 1) or B2 (Band 2). The second field identifies the status indication (refer to Table 13-2). Each line is displayed in one of three colors to indicate the status. Green indicates the band is operating without any faults. Amber indicates the band is degraded but is still operating. Magenta indicates the band is not operational.

13-36. On the PACS menu display selecting the ICS DCL (see Figure 13-2 detail C) will remove the ICMS status displays from the PACS A/A display. Also, if buffer storage becomes critical the ICMS status data will not be displayed.

13-37. The Central Computer (CC) will continuously monitor the communication status of the ICMS. If the CC determines that there has been no valid communication with the ICMS for greater than one second, or the CC has not received a valid checksum for more than one second, the CC shall consider the ICMS status information to be no longer valid and will display OFF in the status field. The status information shall continue to be invalid until the CC receives a valid status message from the ICMS. If there is a power interruption of enough length, the CC will assume that the ICMS status information is invalid until it receives a valid status message and checksum from the ICMS. During that time the CC will continue to display the last known valid status data.

13-38. During airborne flight with the ICMS in manual or auto mode, the ICMS indicates which targets are jammed. On the TEWS LRU 9 display the targets are displayed with an open X around them (see Figure 13-2 detail D). If jamming is not correlated to a target the open X will appear at the center of the display.

13-39. **Power Distribution Band 1 and 2.** See Figure 13-4. The ICMS operates using 115VAC, 3 phase, 400 Hz for primary power and 28VDC for power control. Primary power is provided through a separate group of three circuit breakers for each set. Each set is independent of the other. The 28VDC controls power turn-on for sets 2 and 3. The power function of set 2 is used for explanation. Set 3 power functions are identical.

13-40. Control of ICMS power application is determined by the GND PWR control panel 4 switch position. With the switch in ON position, the ICMS operates from external power as controlled by the TEWS control panel ICS ON/OFF switch. When the engine driven generator comes on the line or external power is removed, the GND PWR control panel 4 switch automatically returns to AUTO. With external power applied to the aircraft and the GND PWR control panel 4 switch in AUTO, no power is applied to the ICMS.

13-41. Primary Power. Primary power is routed to the deenergized contacts of standby relay 2A1K1 and operate relay 2A1K2 in the RF Amplifier, Phase C of primary power is also applied to the coil of standby relay 2A1K1 ICMS power on is done by setting the ICS ON/OFF switch on the TEWS control panel to ON. The ICMS ON signal (ground) energizes standby relay 2A1K1 applying primary power to the elapsed time meter and low voltage power supply within the RF Amplifier. Primary power is also routed through the RF Amplifier to the oscillator. The ICMS ON signal originates in the no. 8 miscellaneous relay panel. The 28VDC from ICS CONT circuit breaker (69CBF021) is routed through the ICS ON/OFF switch to enable the ICS POWER relay on the no. 8 miscellaneous relay panel. The ICS POWER relay applies the ICMS on signal (a ground in the no. 8 miscellaneous relay panel) to the avionics miscellaneous modular relay panel no. 10. The 28VDC from the GND PWR/RUD WRN circuit breaker (54CBE011) is routed to the avionics miscellaneous modular relay panel no. 10 to enable K7 and K8. The output is applied through the oscillator to standby relay 2A1K1 in the RF Amplifier. The 28VDC applied to the ICS POWER relay is also applied to the Avionics Air Circuit Controller to indicate that additional cooling is required.

13-42. RF Amplifier. The RF Amplifier has three separate power supplies, a low voltage power supply, driver TWT power supply and final TWT power supply. When primary power is applied to the input rectifiers, the low voltage power supply is energized. the voltage power supply sends system operating

LEGEND

1 INTEGRATED WITH, BUT NOT PART OF ICMS.
2 EXTERNAL PLUG-IN MODULE.
3 REFER TO TABLE 13-2 FOR CONFIGURATION.
4 68R870053 BALLAST IS INSTALLED WHEN APPLICABLE RF AMPLIFIER/OSCILLATOR IS NOT INSTALLED.
5 ICS RF AMPLIFIER STOWAGE BRACKET INSTALLED WHEN BAND 3 RF AMPLIFIER (FWD) NOT INSTALLED.

INDEX NO.	COMMON NAME	REF DES	S/S/SN	ACCESS
1	SUMMING NETWORK	69E-K010	99-13-20	NO. 5 EQUIPMENT COMPARTMENT
2	SET 3 RF AMPLIFIER OR 4 BALLAST	69ARK003	99-13-17	NO. 5 EQUIPMENT COMPARTMENT
3	SET 3 OSCILLATOR OR 4 BALLAST	69Y-K006	99-13-16	NO. 5 EQUIPMENT COMPARTMENT
4	SET 2 OSCILLATOR OR 4 BALLAST	69Y-K005	99-13-16	NO. 5 EQUIPMENT COMPARTMENT
5	BAND 3 OSCILLATOR	69Y-K025	99-13-32	NO. 5 EQUIPMENT COMPARTMENT
6	SET 2 RF AMPLIFIER OR 4 BALLAST	69ARK002	99-13-18	NO. 5 EQUIPMENT COMPARTMENT
7	BAND 3 RF AMPLIFIER (FWD) OR ICS AMPLIFIER STOWAGE BRACKET 5	69ARK024	99-13-31	NO. 5 EQUIPMENT COMPARTMENT
8	BAND 3 WAVEGUIDE (GROUP)			
	WAVEGUIDE (PULSE)	69W-K518	99-13-40	NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE (CW)	69W-K517	99-13-39	NO. 5 EQUIPMENT COMPARTMENT
	MAGIC TEE	69W-K519	99-13-41	NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE	69W-K520	99-13-42	NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE	69W-K521	99-13-43	COCKPIT
	WAVEGUIDE	69W-H522	99-13-44	COCKPIT
	WAVEGUIDE	69W-H523	99-13-45	COCKPIT
	WAVEGUIDE	69W-A524	99-13-46	FORWARD NOSE BARREL
	WAVEGUIDE	69W-A525	99-13-47	FORWARD NOSE BARREL
	COAX ADAPTER	69W-A526	99-13-48	FORWARD NOSE BARREL
	WAVEGUIDE	69W-G511	99-13-49	NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE	69W-D515	99-13-50	NLG WHEELWELL AND FORWARD NOSE BARREL
	WAVEGUIDE	69W-D512	99-13-51	NLG WHEELWELL AND FORWARD NOSE BARREL
	WAVEGUIDE	69W-B503	99-13-52	FORWARD NOSE BARREL
	WAVEGUIDE	69W-B504	99-13-38	FORWARD NOSE BARREL
9	SET 2 ANTENNA (CENTER)	69E-D008	99-13-14	FORWARD NOSE BARREL
10	BAND 3 FWD UP ANTENNA	69E-B031	99-13-35	FORWARD NOSE BARREL
11	CABLE ASSEMBLY (FWD UP)	69W-A527	99-13-53	FORWARD NOSE BARREL
12	BAND 3 FWD DOWN ANTENNA	69E-B037	99-13-36	FORWARD NOSE BARREL
13	CABLE ASSEMBLY (SET 2)	69W-K509	99-13-22	NOSE BARREL AND NO. 5 EQUIPMENT COMPARTMENT
14	WAVEGUIDE (GROUP) SET 2			
	WAVEGUIDE	69W-G513	99-13-27	NLG WHEELWELL AND NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE	69W-D516	99-13-30	MLG WHEELWELL
	WAVEGUIDE	69W-D514	99-13-24	FORWARD NOSE BARREL
15	CABLE ASSEMBLY, SET 3	69W-K510	99-13-23	ECS BAY AND NO. 5 EQUIPMENT COMPARTMENT

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Figure 13-1. Countermeasures Set AN/ALQ-135E/(V)
(Sheet 1 of 8)

INDEX NO.	COMMON NAME	REF DES	S/S/SN	ACCESS
16	WAVEGUIDE (GROUP) SET 3			
	WAVEGUIDE	69W-K506	99-13-25	NO. 5 EQUIPMENT COMPARTMENT
	WAVEGUIDE	69W-N507	99-13-26	ECS BAY
17	SET 3 ANTENNA (AFT)	69E-N009	99-12-12	ECS BAY
18	PROGRAMMER ◀2 ◀3		99-13-19	BAND 1 OSCILLATOR
19	PROGRAMMER ◀2 ◀3		99-13-19	BAND 2 OSCILLATOR
20	BAND 3 AFT ANTENNA	69E-T033	99-13-37	RIGHT HAND TAIL CONE AND DOOR 129R
21	CABLE ASSEMBLY (PULSE-AFT)	69W-T531	99-13-57	RIGHT HAND TAIL BOOM
22	CABLE ASSEMBLY (CW-FWD)	69W-T529	99-13-55	DOOR 116R
23	COAX ADAPTER (CW)		99-13-58	DOOR 116R
24	COAX ADAPTER (PULSE)		99-13-59	DOOR 116R
25	CABLE ASSEMBLY (PULSE-FWD)	69W-T530	99-13-56	DOOR 116R
26	BAND 3 RF AMPLIFIER (AFT) OR ICS RF AMPLIFIER STOWAGE			
	BRACKET ◀5	69ART030	99-13-33	DOOR 116R
27	CABLE ASSEMBLY (CW-AFT)	69W-T528	99-13-54	RIGHT HAND TAIL BOOM
28	PREAMPLIFIER	69ART034	99-13-34	DOOR 139
29	TEWS IA CONTROL PANEL	65Z-H011	99-11-15	COCKPIT, LEFT CONSOLE
30	BIT CONTROL PANEL ◀1	65Z-H002	31-50-11	COCKPIT, LEFT CONSOLE
31	AVIONICS STATUS PANEL ◀1	66Z-G001	31-50-10	NLG WHEELWELL
32	GND PWR CONTROL PANEL	52Z-H069	39-10-13	COCKPIT, LEFT CONSOLE
33	TEWS CONTROL PANEL	65Z-J010	99-11-14	COCKPIT, RIGHT CONSOLE
34	RIGHT BUS CIRCUIT BREAKER PANEL NO. 1 ◀1	52Z-F005	24-50-17	DOOR 10R
35	NO. 8 MISCELLANEOUS RELAY PANEL	52Z-L258	39-40-34	NO. 5 EQUIPMENT COMPARTMENT
36	ICS POWER RELAY ◀1	69K-L022	39-40-10	NO. 8 MISCELLANEOUS RELAY PANEL
37	MULTIPURPOSE COLOR DISPLAY ◀1		94-10-27	COCKPIT
38	TEWS DISPLAY UNIT ◀1	65Z-J009	99-11-13	COCKPIT

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Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 2)

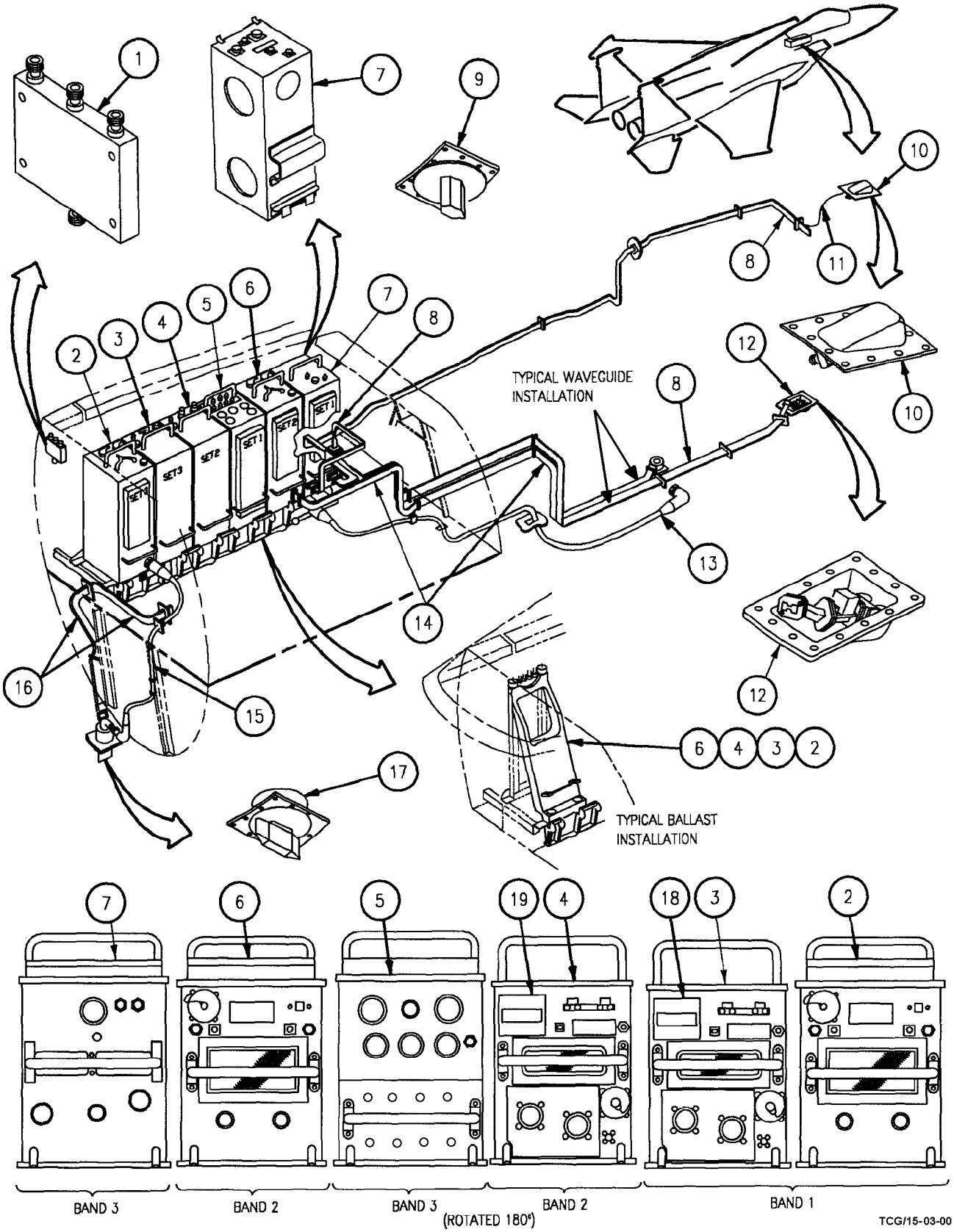


Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 3)

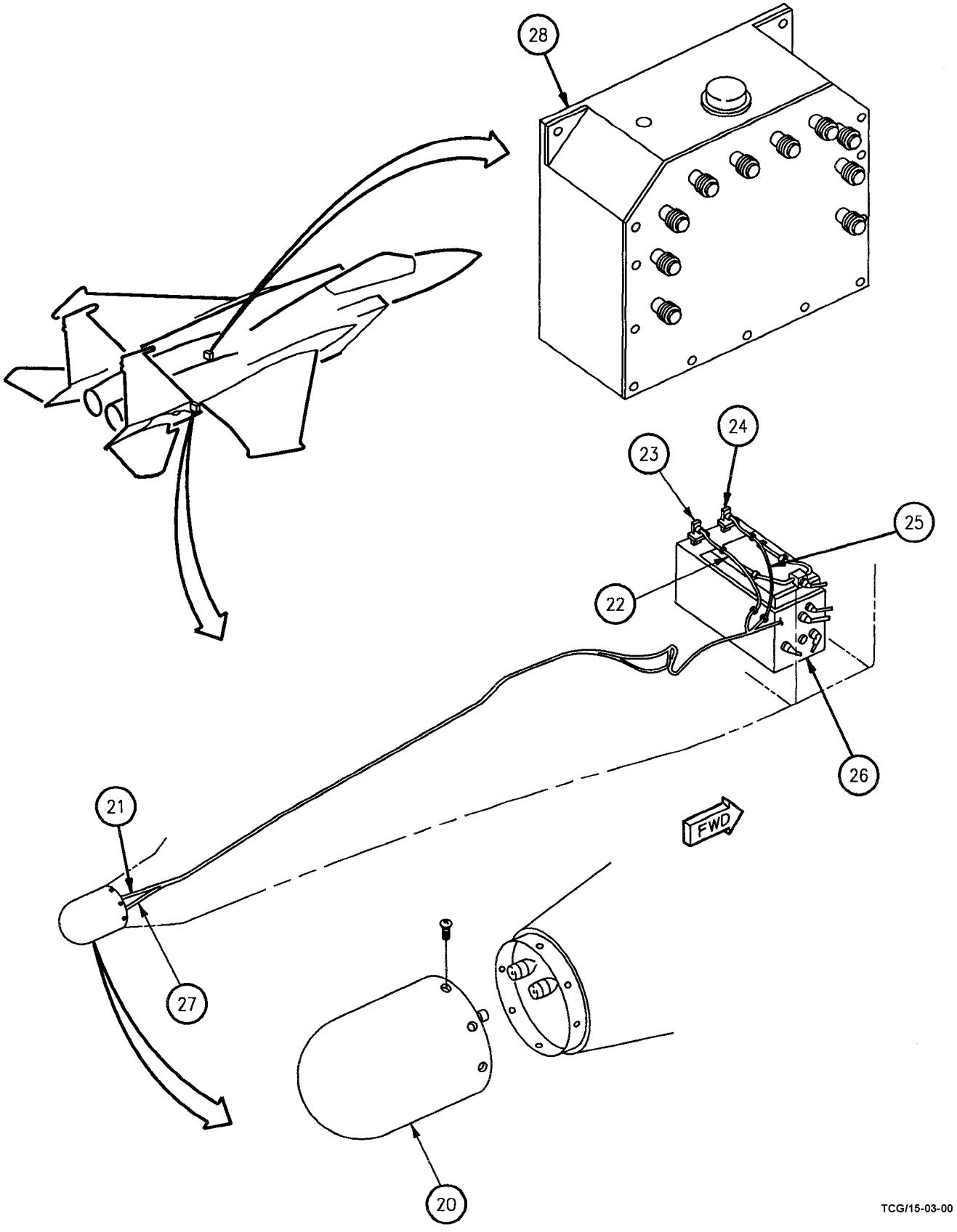
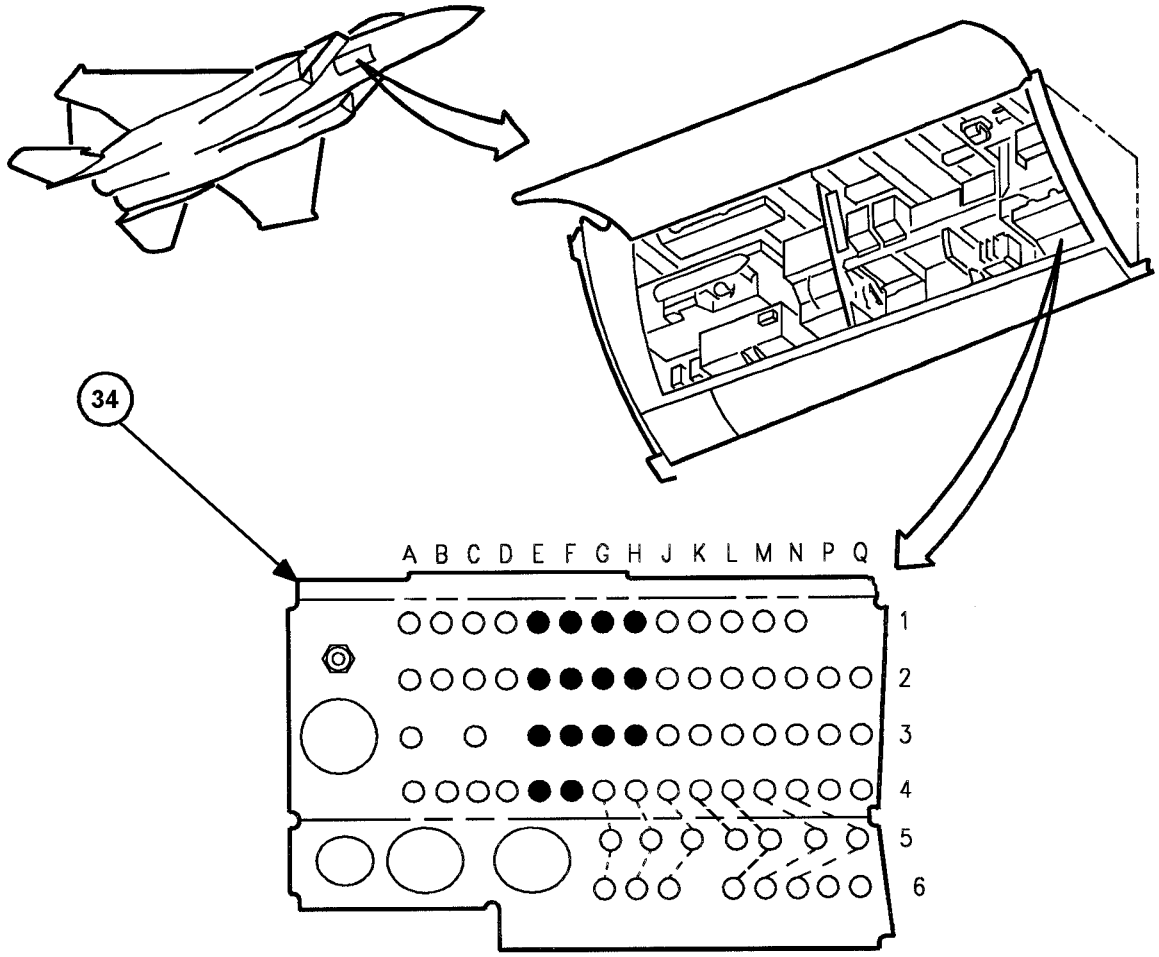


Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 4)



52Z-F005		RIGHT BUS CIRCUIT BREAKER PANEL NO. 1		(24-50-17)
REF DES	ZONE	NOMENCLATURE		BUS
69CBF027	E1	ICS PWR BD 3 AFT	115VAC ϕB	R 115VAC ϕB
69CBF026	E2	ICS PWR BD 3 AFT	115VAC ϕA	R 115VAC ϕA
69CBF028	E3	ICS PWR BD 3 AFT	115VAC ϕC	R 115VAC ϕC
69CBF029	E4	ICS PWR BD 3 AFT	28VDC	R 28VDC
69CBF018	F1	ICS PWR BD 3 FWD	115VAC ϕB	R 115VAC ϕB
69CBF017	F2	ICS PWR BD 3 FWD	115VAC ϕA	R 115VAC ϕA
69CBF019	F3	ICS PWR BD 3 FWD	115VAC ϕC	R 115VAC ϕC
69CBF021	F4	ICS CONT	28VDC	R 28VDC
69CBF015	G1	ICS PWR BD 1/2	115VAC ϕB	R 115VAC ϕB
69CBF014	G2	ICS PWR BD 1/2	115VAC ϕA	R 115VAC ϕA
69CBF016	G3	ICS PWR BD 1/2	115VAC ϕC	R 115VAC ϕC
69CBF012	H1	ICS PWR BD 1/2	115VAC ϕB	R 115VAC ϕB
69CBF011	H2	ICS PWR BD 1/2	115VAC ϕA	R 115VAC ϕA
69CBF013	H3	ICS PWR BD 1/2	115VAC ϕC	R 115VAC ϕC

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Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 5)

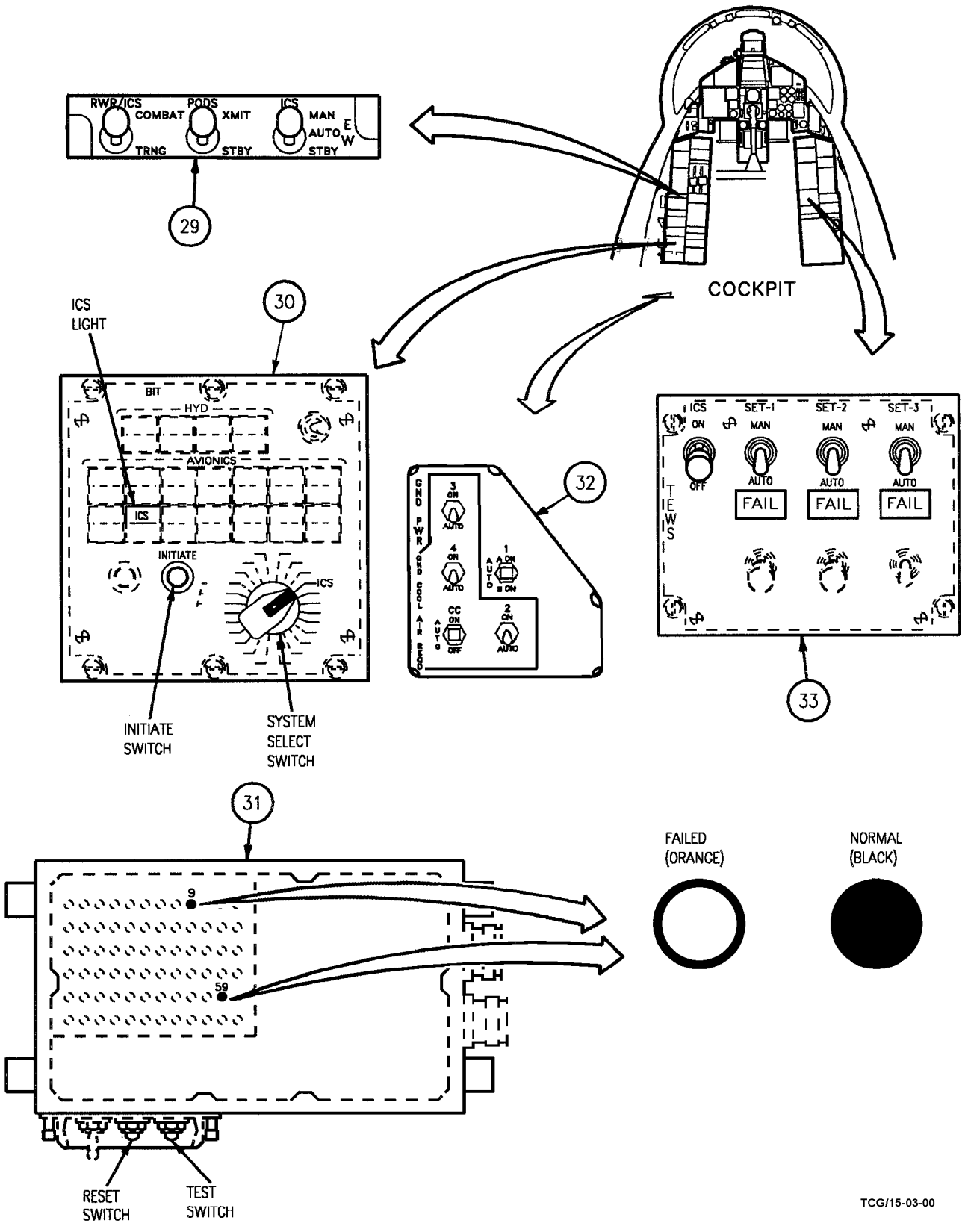
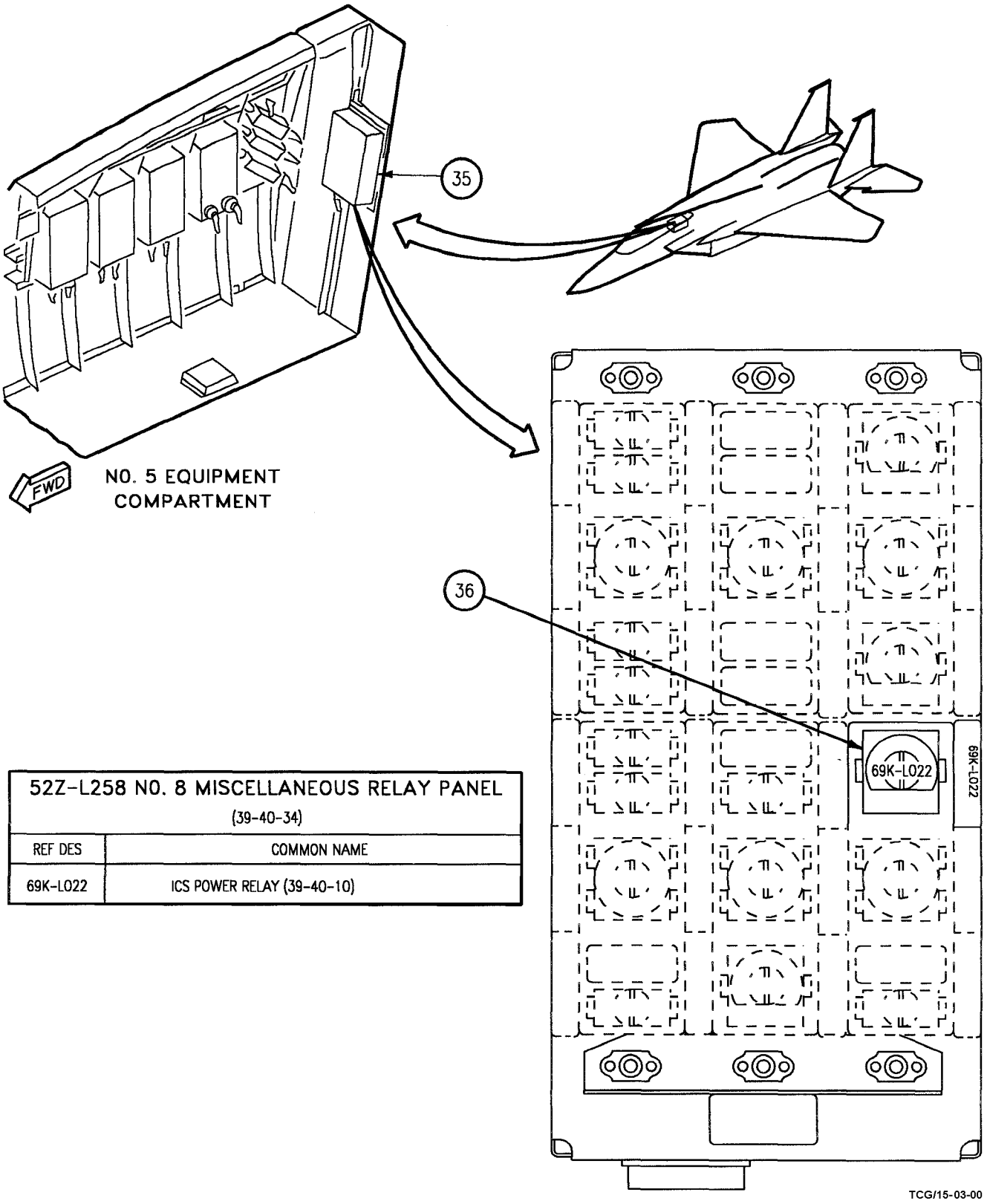


Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 6)



52Z-L258 NO. 8 MISCELLANEOUS RELAY PANEL (39-40-34)	
REF DES	COMMON NAME
69K-L022	ICS POWER RELAY (39-40-10)

Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 7)

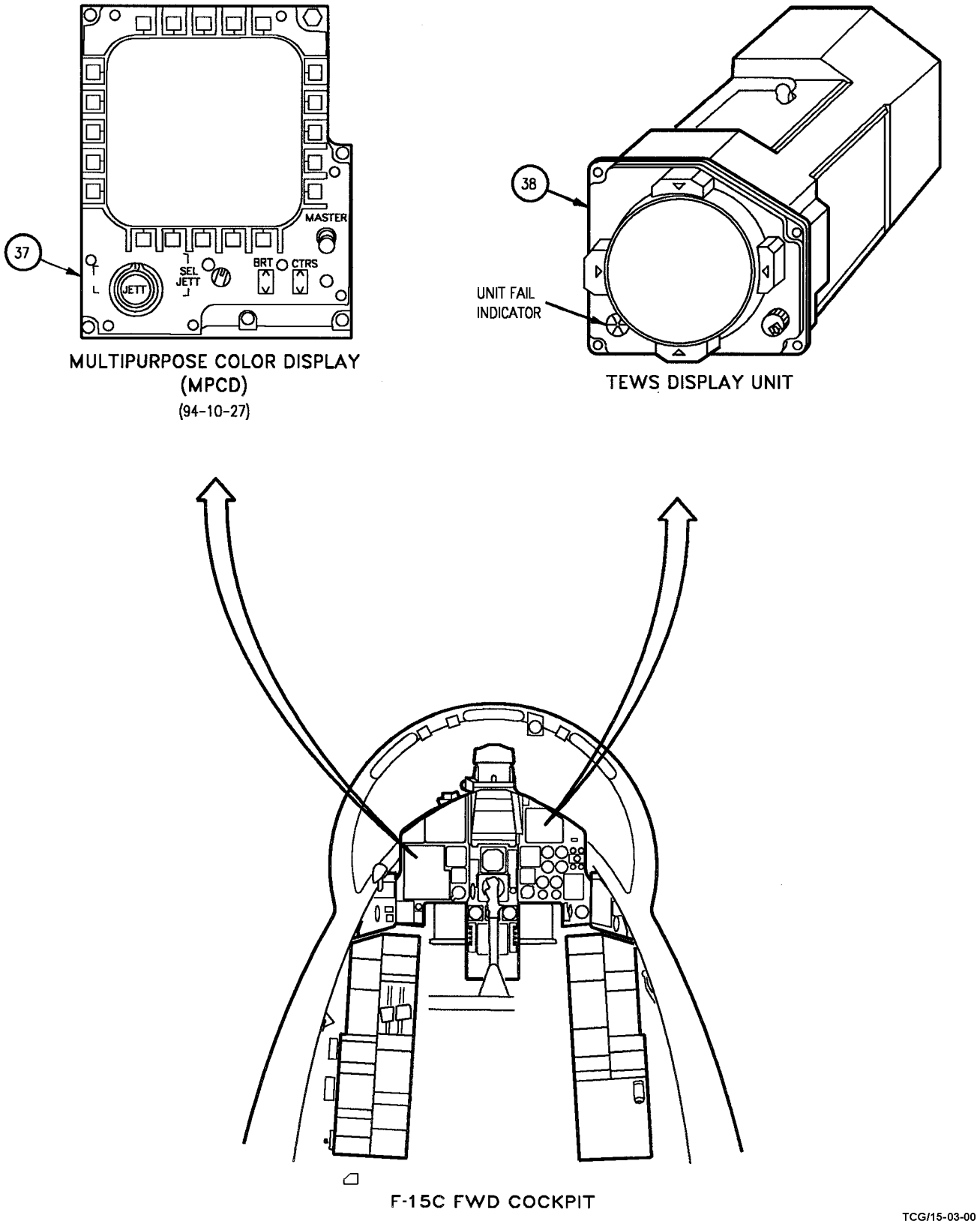


Figure 13-1. Countermeasures Set AN/ALQ-135E/(V) (Sheet 8)

Table 13-3. Controls and Indicators

Control/Indicator	Position/Condition	Function/Indication
RWR ON/OFF switch	ON	a. Enables 115VAC, 400 Hz, 3Ø and +28VDC aircraft power application to RWR. b. Applies an RWR ON signal to ICMS, indicating to lCMS that RWR is on and will receive and/or transmit lCMS programmed data.
	OFF	a. Removes RWR system power. b. Disables RWR and ICMS data communication.
ICS ON/OFF switch	ON	Enables 115VAC, 400 Hz, 3Ø and +28VDC aircraft power application to ICMS.
	OFF	a. Removes ICMS system power b. Keeps relay K1, in TEWS control panel, energized enabling a reduced (10%) cooling air application to ICMS.
SET-1, SET-2, SET-3 switches	AUTO	Enables the selected ICMS set to be controlled by RWR when ICS MAN/ AUTO/STBY switch on TEWS IA control panel is in MAN or AUTO.
	MAN	Enables a selected ICMS set to be controlled independently when ICS MAN/AUTO/STBY switch on TEWS IA control panel is in MAN.
SET-1 FAIL, SET-2 FAIL, SET-3 FAIL lights	On	Indicates a failure in selected ICMS transmitting set.
	Not on	Indicates selected ICMS transmitting set is operating correctly.
TEWS IA Control Panel		
RWR/ICS switch	COMBAT	Allows AUTO mode operation of ICMS.
	TRNG	Enables ICS training mode (inflight only). Inhibits ICMS AUTO mode of operation.

Table 13-3. Controls and Indicators (CONT.)

Control/Indicator	Position/Condition	Function/Indication
ICS MAN/AUTO/STBY switch	MAN	Enables jamming modes (MAN or AUTO) to be selected by SET-1, 2, or 3 switches on TEWS control panel.
	AUTO	ICMS sets are maintained in auto mode and controlled by the RWR.
	STBY	Puts all ICMS sets in STBY mode.
BIT Control Panel		
System select switch	ICS	In ICS position selects ICMS system when manual BIT is to be done.
INITIATE	Pressed and released	Enables ICMS BIT program.
ICS light	On (steady)	a. When ICMS is off and external electrical power is applied to aircraft.
		b. For 5 minute warmup, when ICMS is enabled.
		c. When ICMS is on and system failure occurs.
	Flashing	During period of BIT program.
	Not on	When ICMS is on and operational.
GND Control Panel		
Switch #4	AUTO	Disables application of external power to ICMS.
	ON	Enables application of external power to ICMS.
Multipurpose Color Display		
Detail BIT display (accessed from BIT 1 display)		
S15 (TEWS)	Press and release	Enables TEWS detail BIT display.
TEWS detail BIT display (accessed from detail BIT display)		
S4 (ICS BIT LOG)	Press and release	Enables ICMS BIT log display.
S6 (RWR)	Press and release	Enables RWR functional fault display.
S7 (ICS)	Press and release	Enables ICMS functional fault display.

Table 13-3. Controls and Indicators (CONT.)

Control/Indicator	Position/Condition	Function/Indication
ICMS detail BIT display (accessed from TEWS detail BIT display)		
S7 (ICS)	Press and release	Will be displayed in the ICMS detail BIT display to indicate ICMS detail BIT data is being provided.
S11 (MENU)	Press and release	Enables menu 1 display.
S15 (TEWS)	Press and release	Enables the detail BIT display.
NO DATA AVAILABLE	Displayed	Displayed in the first functional failure position when the CC recognizes a previous ICMS software version, or when CC to ICMS communication cannot be established.
NO ICS/CC 1553 COM	Displayed	Displayed in the first functional failure position when the ICMS/CC communication has either never been established on the 1553 data bus, or has been established on the H009 data bus.
ICMS BIT LOG display (accessed from TEWS detail BIT display)		
S4 (ICS BIT LOG)	Press and release	Enables ICS BIT log display. Pressing S4 again will return to TEWS detail BIT display.
S13/S14	Press and release	Toggling between S13 and S14 allows paging up or down through ICMS BIT LOG data.
S11 (MENU)	Press and release	Return to menu 1.
S15 (TEWS)	Press and release	Return to detail BIT display.
NO DATA AVAILABLE	Displayed	This indication will be displayed if no data is available or an error exists with transfer of ICMS BIT log data in weight-on-wheels condition.
Air Navigation Multiple Indicator		
Air-to-Air radar display		
FCR (Fire Control Radar) Desensitization Cue	Displayed	a. The radar desensitization cue displayed in the upper left corner of the display in the large character set and displayed at full intensity.

Table 13-3. Controls and Indicators (CONT.)

Control/Indicator	Position/Condition	Function/Indication
		b. The radar desensitization cue is displayed on the air to air radar display when the radar is operating in Track While Scan (TWS) range H, M, or I. c. The desensitization cue represents the relative sensitivity (i.e. detection range) of the radar. d. The desensitization cue shall be displayed as a value ranging from 1 to 4.

Table 13-4. Band 1 and 2 Status Field Displays

Display	Description
OFF	B2 OFF indicates Band 2 via the RWR is not communicating with the CC. B1 OFF indicates Band 1 via the RWR is not communicating with the CC.
NOP	Band 1 or 2 not operational
DGR	B2 DGR indicates that the Band 2 performance is degraded. B1 DGR indicates that the Band 1 performance is degraded.
JAM	B2 JAM indicates that Band 2 is jamming one or more targets. B1 JAM indicates that Band 1 is jamming one or more targets.
AUT	ICMS is in auto mode.
MAN	Band 1 or 2 in manual mode.
Status is listed in order from highest to lowest priority.	

Table 13-5. Band 3 Status Field Displays

Display	Description
OFF	B3 OFF indicates the Band 3 is not communicating with the CC, or the communication is not valid.
WRM	Band 3 is warming up.
BIT	Band 3 is running built-in test.
INI	Band 3 is initializing.
NOP	Band 3 not operational.

Table 13-5. Band 3 Status Field Displays (CONT.)

Display	Description
TMP	Band 3 amp is exceeding operating temperature.
DGR	B3 DGR indicates that the Band 3 performance is degraded.
	NOTE When a radar special mode has been activated, the ICMS inhibits jamming forward and aft within the inhibit bandwidth. The ICMS status display will still indicate JAM (if JAM was already displayed) for the complete duration that the radar special mode is activated.
JAM	B3 JAM indicates that Band 3 is jamming one or more targets.
AUT	ICMS is in auto mode.
STB	B3 STB indicates that Band 3 is in standby.
MAN	Band 3 in manual mode.
Status is listed in order from highest to lowest priority.	

Table 13-6. Band 3 Limitation Field Displays

Display	Description
F/A	When displayed with TMP in the status field, forward and aft jamming is lost. When displayed with DGR in the status field, forward and aft jamming is degraded.
FWD	Forward jamming degraded or lost.
AFT	Aft jamming degraded or lost.
CAL	Jamming degraded due to chop calibration failure (valid only with DGR in the status field).
COR	Jamming correlation with RWR is lost (valid only with DGR in status field).
	Band 3 degradation not aspect related (valid only with DGR in the status field).
Limitations listed in order from highest to lowest priority.	

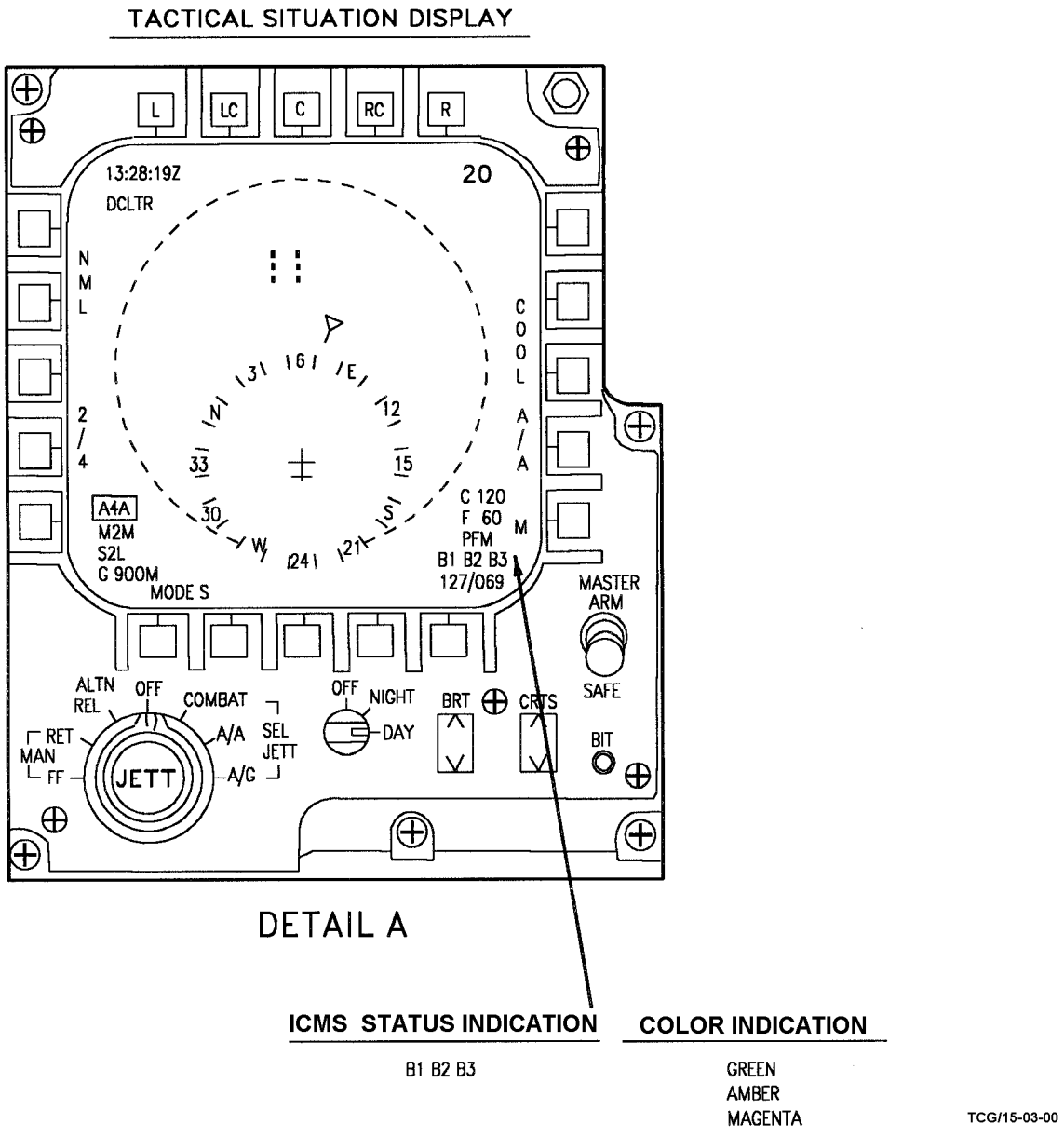


Figure 13-2. ICMS Displays (Sheet 1 of 4)

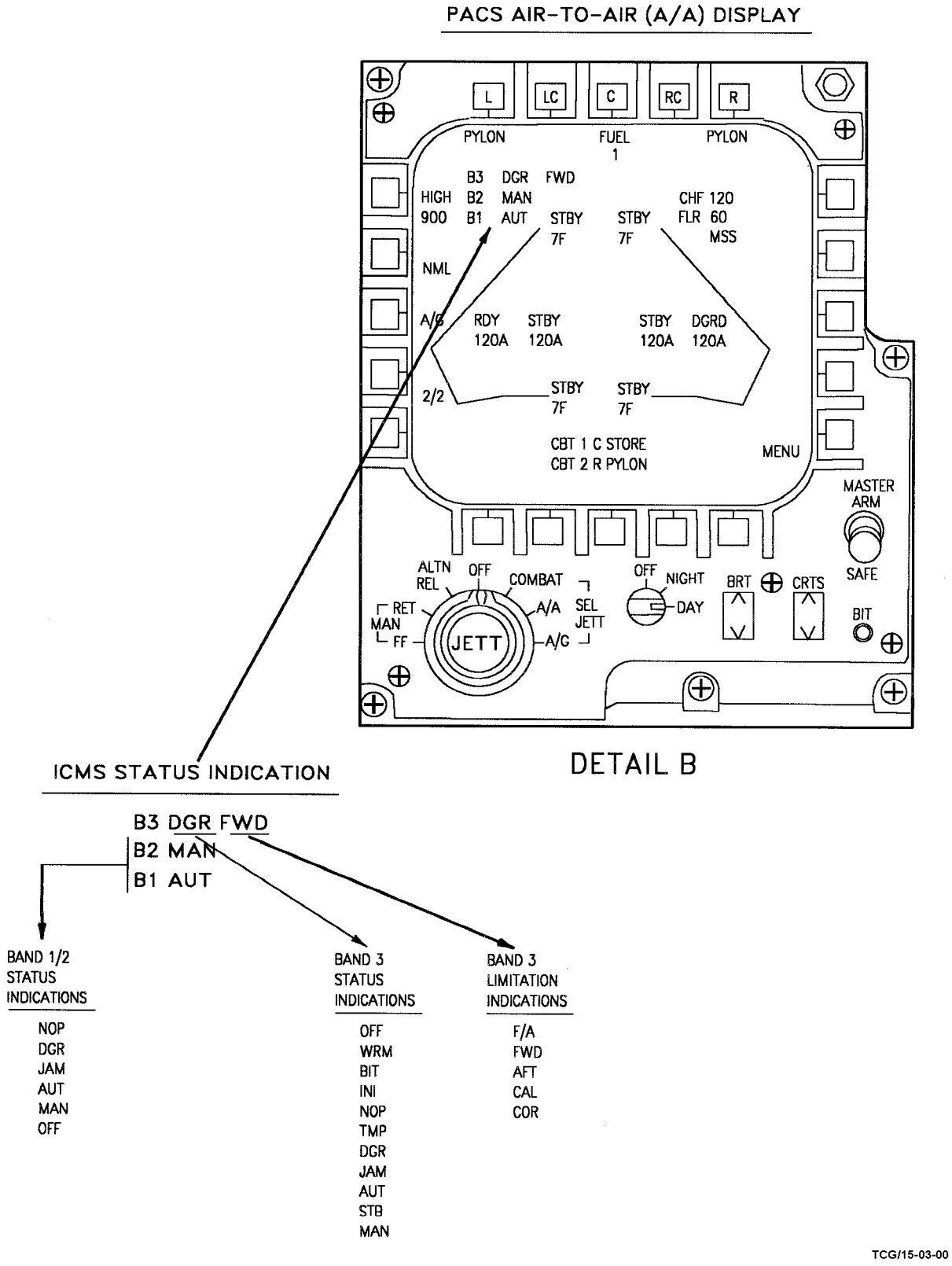
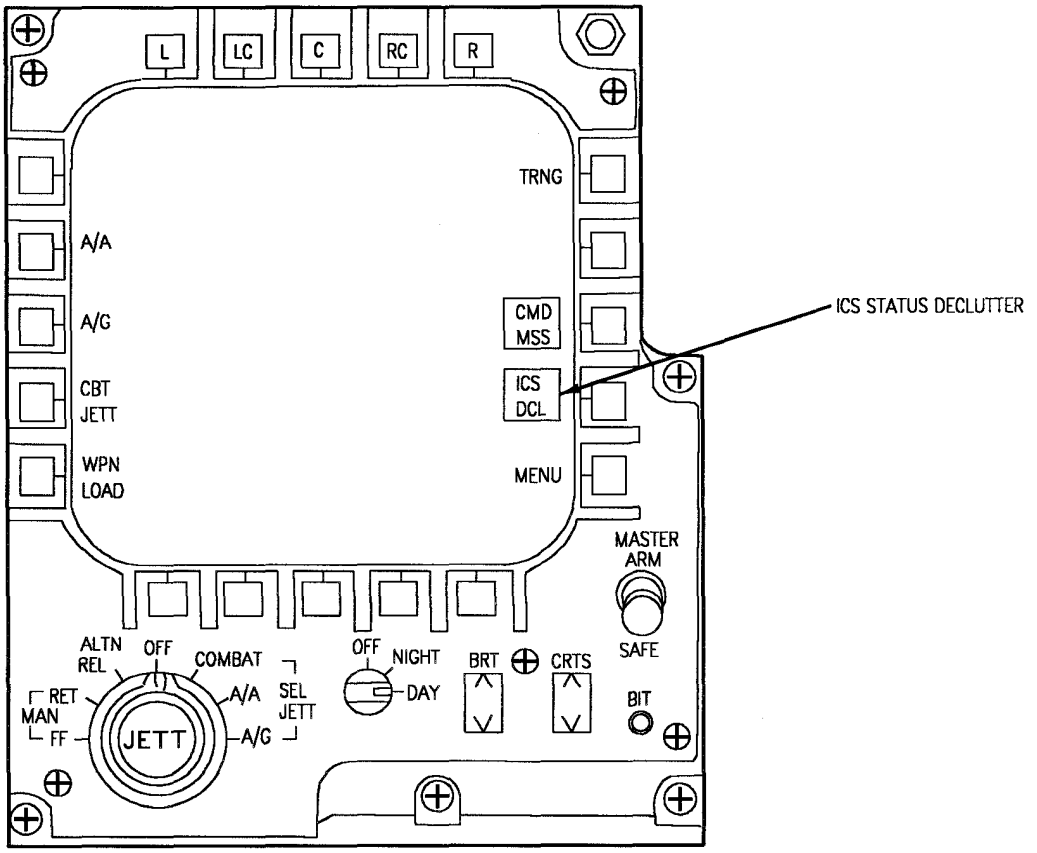


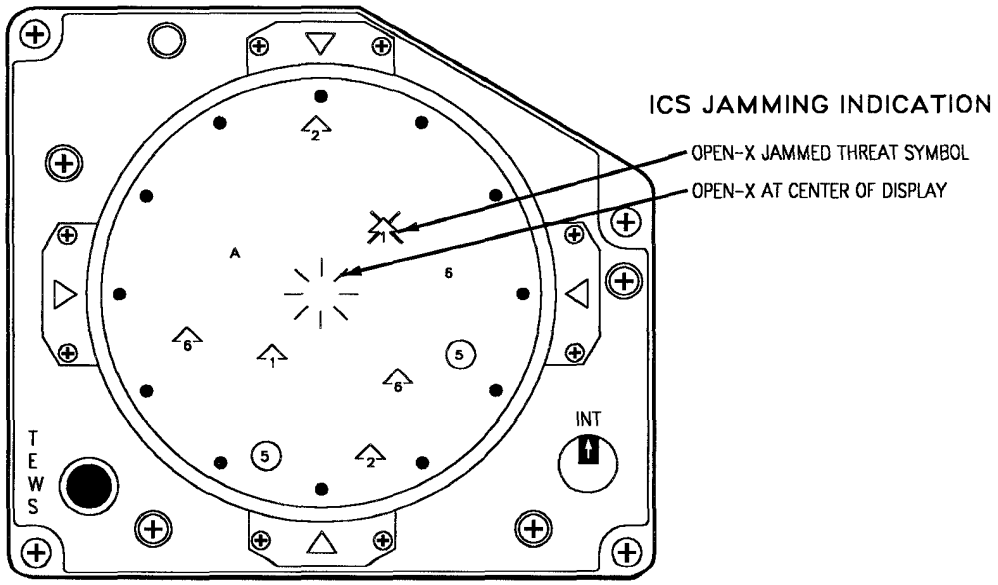
Figure 13-2. ICMS Displays (Sheet 2)

PACS MENU DISPLAY



DETAIL C

TEWS LRU-9 DISPLAY



DETAIL D

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Figure 13-2. ICMS Displays (Sheet 3)

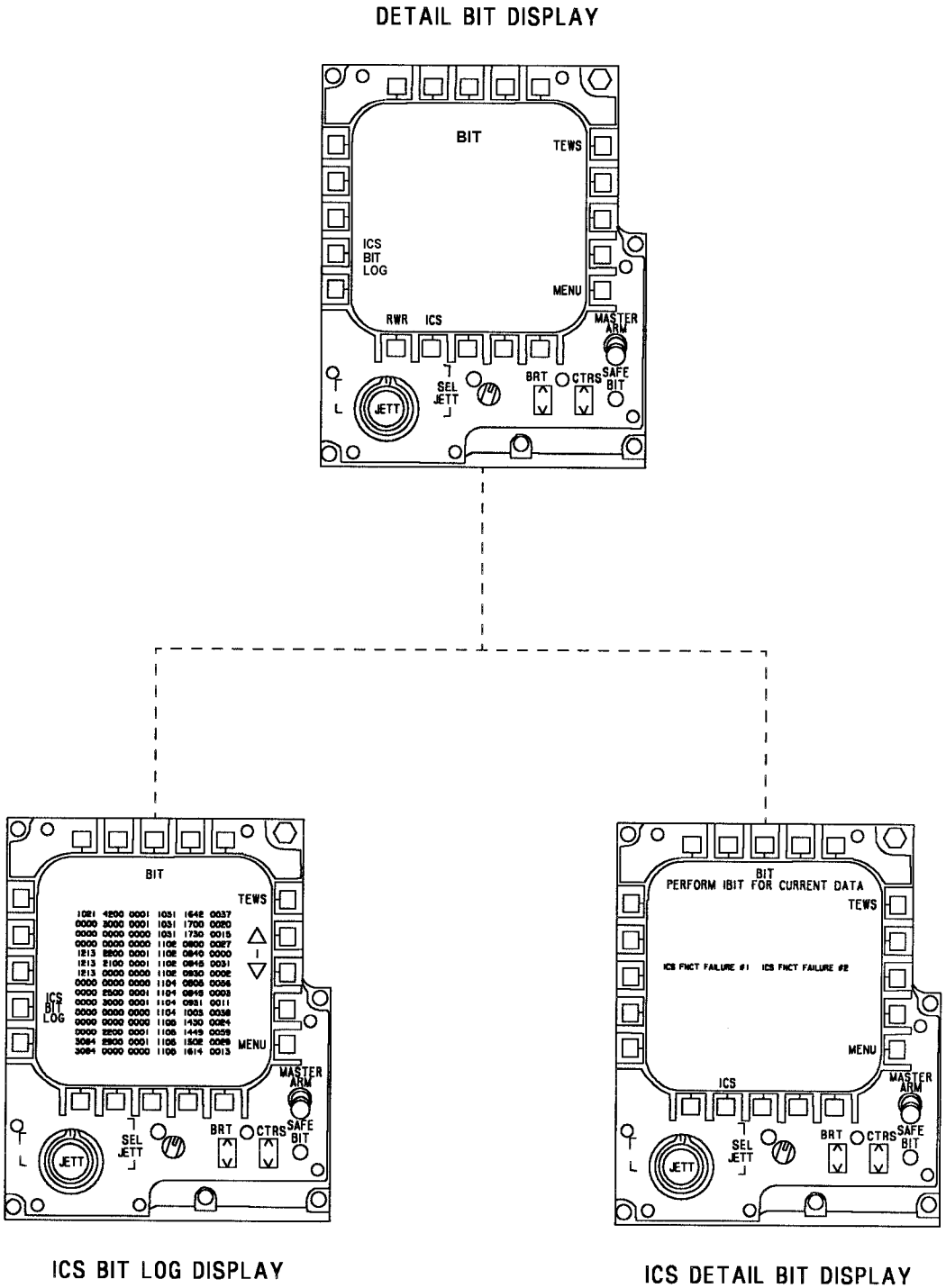

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Figure 13-2. ICMS Displays (Sheet 4)

voltages to the driver TWT power supply, final TWT power supply, modulator, automatic level control, and set control modules. Twelve volts DC is also applied to the coil of operate relay 2A1K2 and routed to the oscillator for use by the interface module. The driver TWT power supply and the final TWT power supply, when enabled, provide operating voltages to the driver TWT and final TWT. Both of these power supplies send fail signals to the BIT circuitry if a failure occurs. When operating voltages are applied to the set control module, a 5 minute cycle-in timer is enabled. This starts a 5 minute system warmup period. At the end of the 5 minute time out, a CYCLE-IN GATE is produced. The CYCLE-IN GATE signal is sent to the oscillator low voltage power supply and fault locator. The fault locator supplies the BIT NO GO signal which illuminates the ICS light on the BCP during system warmup. When the warmup cycle is completed, the CYCLE-IN GATE signal applied to the fault locator holds relay K4 on the fault detection module energized, turning off the ICS light on the BCP, indicating the system has completed warmup. All three power supplies are monitored for out of tolerance conditions and are disabled if a failure occurs.

13-43. Oscillator. The low voltage power supply in the oscillator has two different DC supplies; the standby power supply and the operate power supply. Both supplies provide DC operating voltages for the oscillator. When three-phase power from the RF Amplifier is available at the input, the standby power supply, tuning unit heaters and elapsed time meter are energized. The standby power supply provides 28VDC to the coil of relay A3A1K1 and also routes 28VDC to the RF Amplifier for use by the BIT indicators. Each tuning unit has two blanket heaters; a 25 watt heater and a 100 watt heater. Primary power is applied directly to the 25 watt heater and passes through the normally closed contacts of relay A3A1K1 to the 100 watt heater. Relay A3A1K1 is energized after the 5 minute warmup when the CYCLE-IN GATE signal becomes active and no failures exist. Energizing relay A3A1K1 removes primary power from the 100 watt heater and also removes ground applied to the operate switch drive, allowing the power supply to be enabled when the OPERATE COMMAND becomes active. The operate power supply is enabled when the OPERATE COMMAND or a BIT INITIATE signal is available and no failures exist. Both supplies are monitored for BIT reasons and are disabled if a failure occurs. If the operate power supply is disabled the system returns to a standby condition. If the standby power supply is disabled the system is shut down and the ICS light remains on.

13-44. **Control Circuits.** See Figure 13-5. The ICMS power on and mode control is done through switch controls on the TEWS control panel and TEWS IA control panel. The ICMS may be operated in manual, auto, or standby mode. Also, each set may be operated separately in either manual or auto mode. When the ICMS is off, ICMS relay K1 in the TEWS control panel is energized by a ground applied through the ICS ON/OFF switch. Energizing ICS relay K1 reduces the ECS cooling air flow to the ICMS. The amount of ECS cooling air flow to the ICMS is controlled by the ICMS cooling control valve which is energized by the ICMS 10% COOLING signal. The ICMS 10% COOLING signal is a 28VDC signal routed from right bus circuit breaker panel no. 1 through ICS relay K1 to the ICMS cooling control valve. When the ICMS is off, 10 percent of the available ECS cooling air is supplied to the system. When the ICMS is on, 100 percent of the available ECS cooling air is supplied to the system. The ICMS cooling control valve operates only with one or both aircraft engines operating. The valve is closed by actuator air pressure (15 psig) from the engine bleed air system when the ICMS is operating in either manual or auto mode. When operating on ground power, the valve is closed only by external air pressure applied through the ICMS cooling control valve test connector.

13-45. Standby Mode. Standby mode is selected by setting the ICS MAN/AUTO/STBY switch on the TEWS IA control panel to STBY. When in standby, the ICMS MODE RTN signal (ground) is routed from the RF Amplifier through the oscillator and ICS MAN/AUTO/STBY switch to the TEWS control panel to energize ICS relay K1. ICS relay K1, when energized, reduces ECS cooling air flow to the ICS system. When STBY is selected, all three ICMS sets are in standby and position of the SET-2 and SET-3 switches on the TEWS control panel has no effect on the system.

13-46. Manual Mode. Manual mode is selected for each set of the ICMS by setting the ICS switch on the TEWS IA control panel to MAN, and setting the respective SET-2 or SET-3 switch on the TEWS control panel to MAN. The two sets may be operated in manual or auto mode, either separately or simultaneously. Manual mode is not recommended because of possible interference with the RWR.

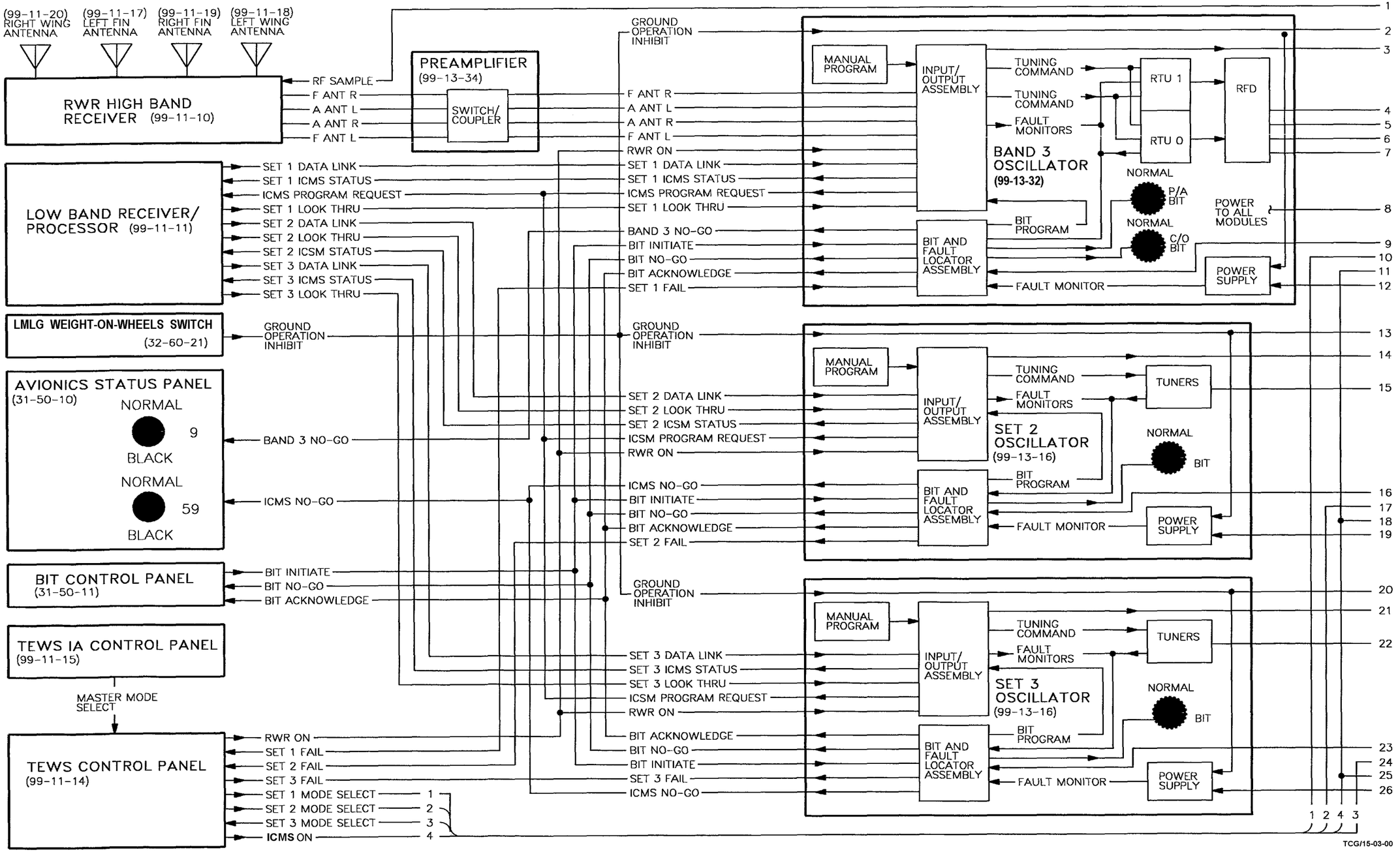

Figure 13-3. ICMS Functional Block Diagram (Sheet 1 of 2)

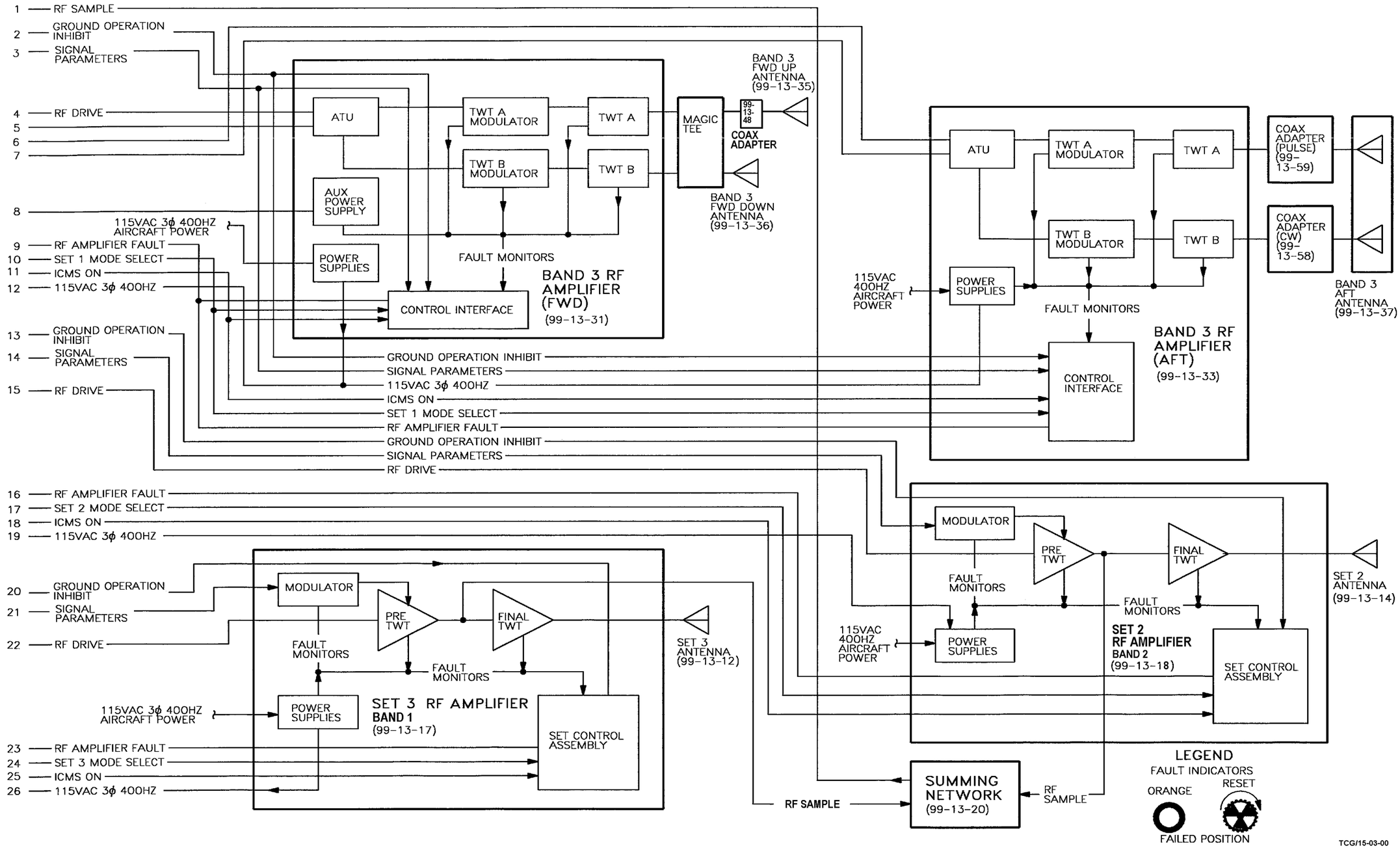

Figure 13-3. ICMS Functional Block Diagram (Sheet 2)

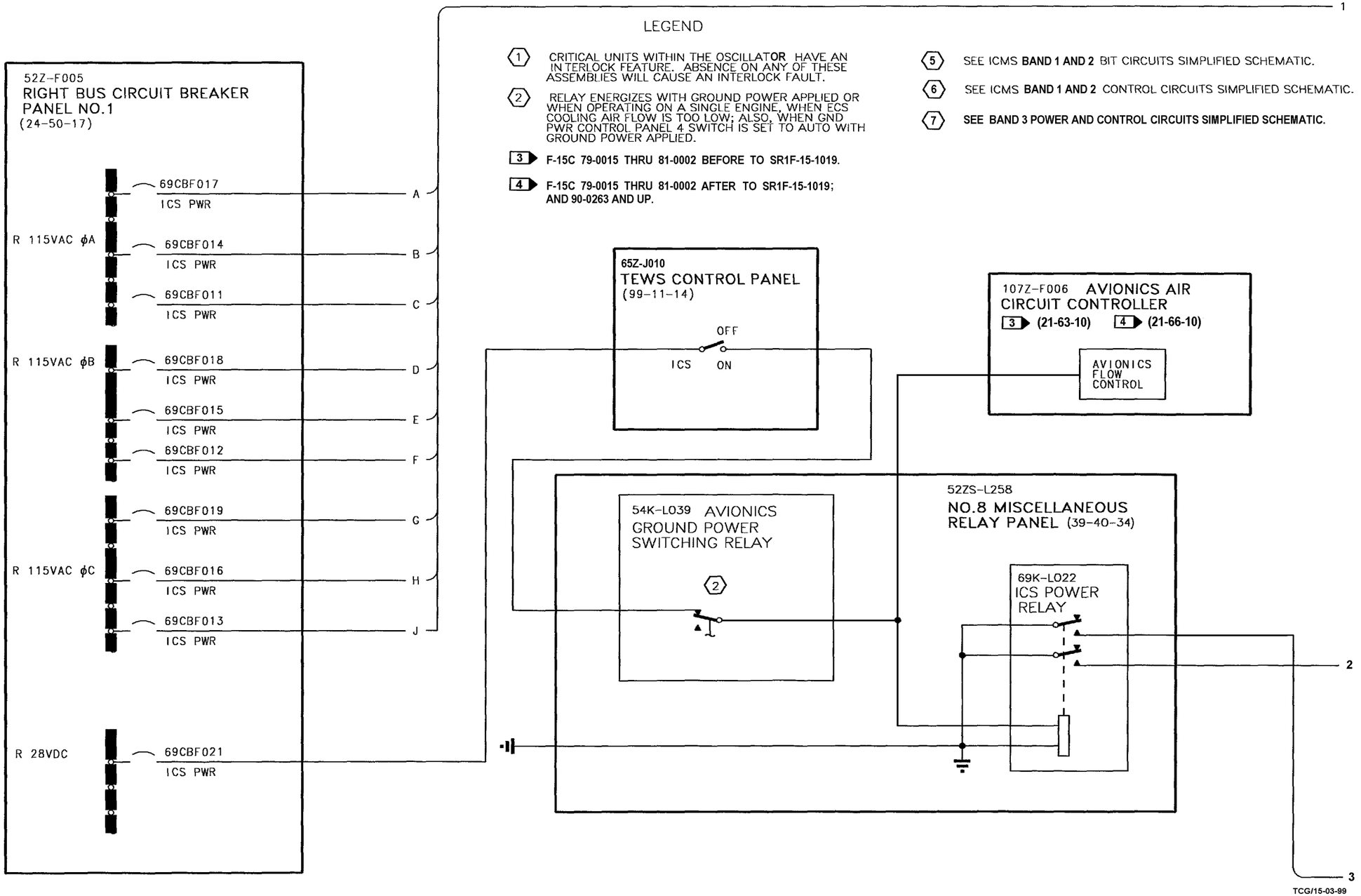

Figure 13-4. ICMS Band 1 and 2 Power Distribution Simplified Schematic (Sheet 1 of 5)

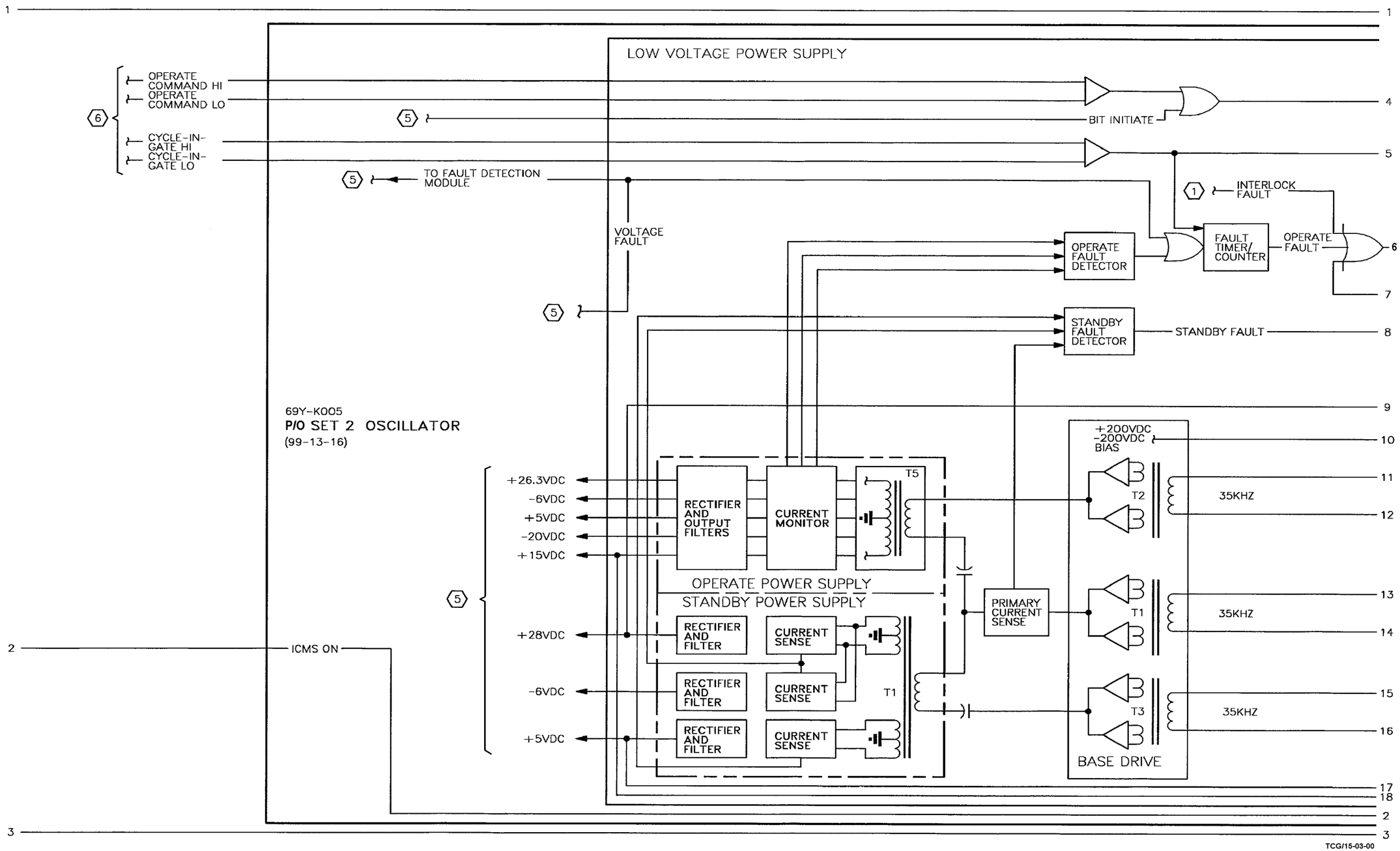

Figure 13-4. ICMS Band 1 and 2 Power Distribution Simplified Schematic (Sheet 2)

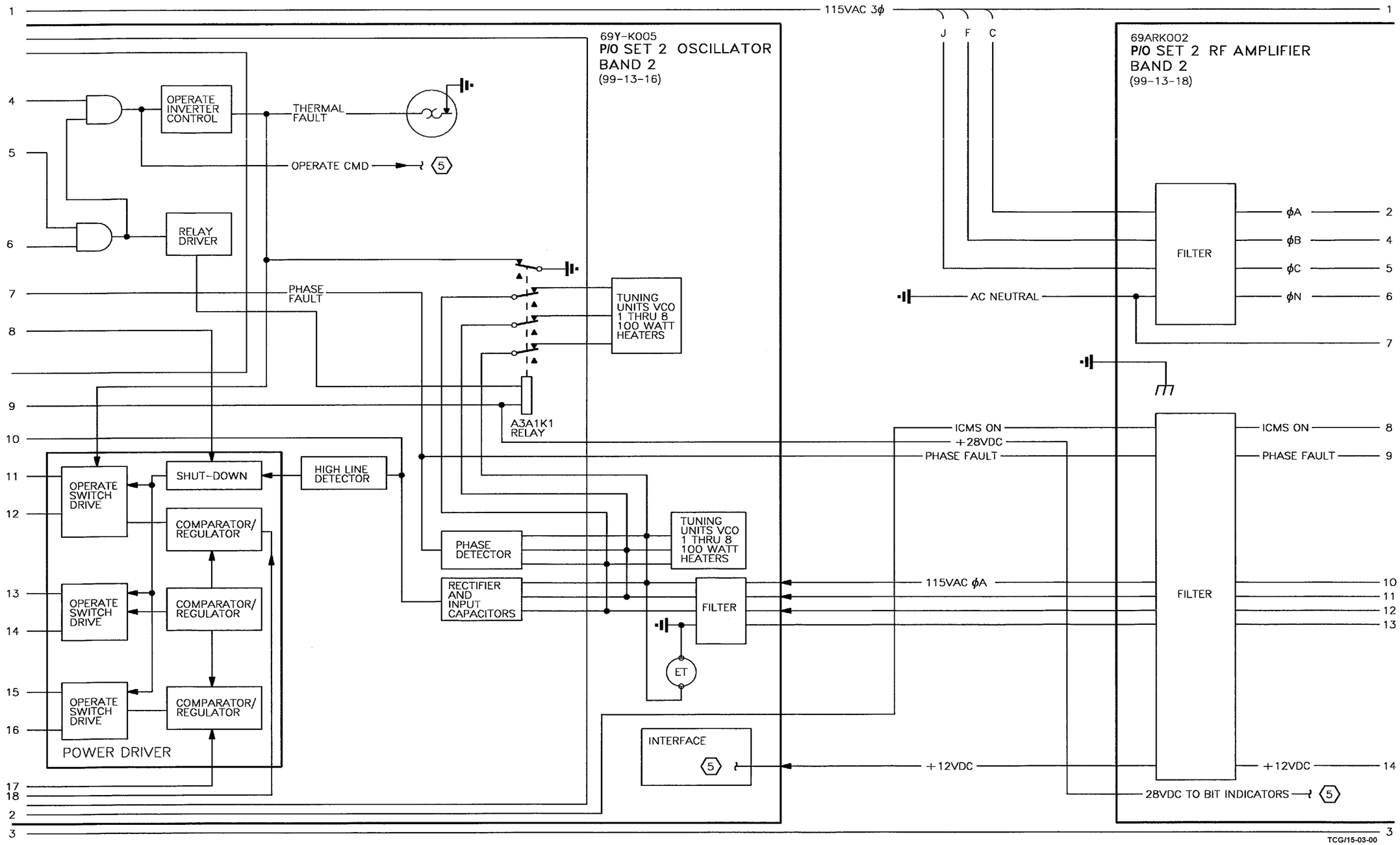

Figure 13-4. ICMS Band 1 and 2 Power Distribution Simplified Schematic (Sheet 3)

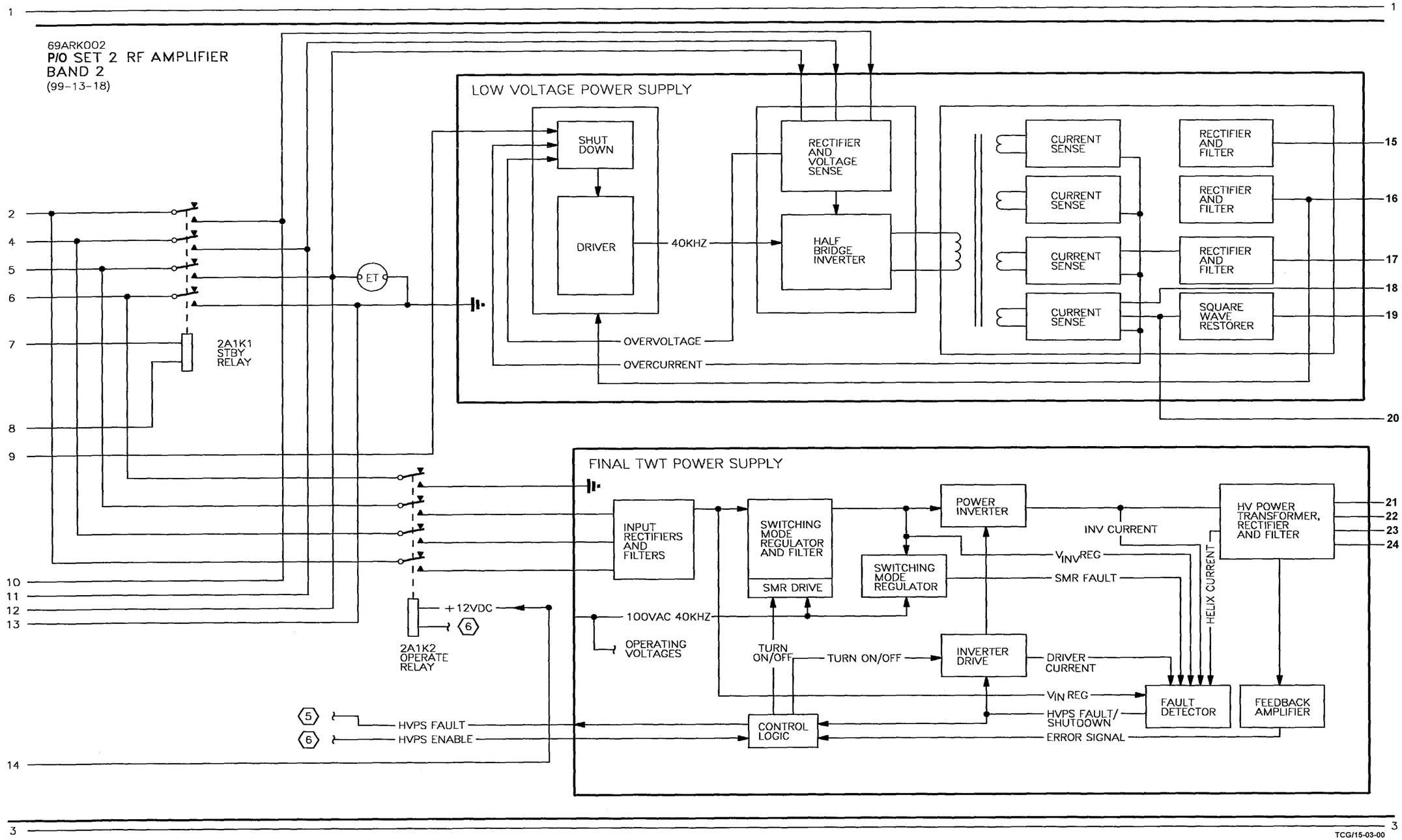

Figure 13-4. ICMS Band 1 and 2 Power Distribution Simplified Schematic (Sheet 4)

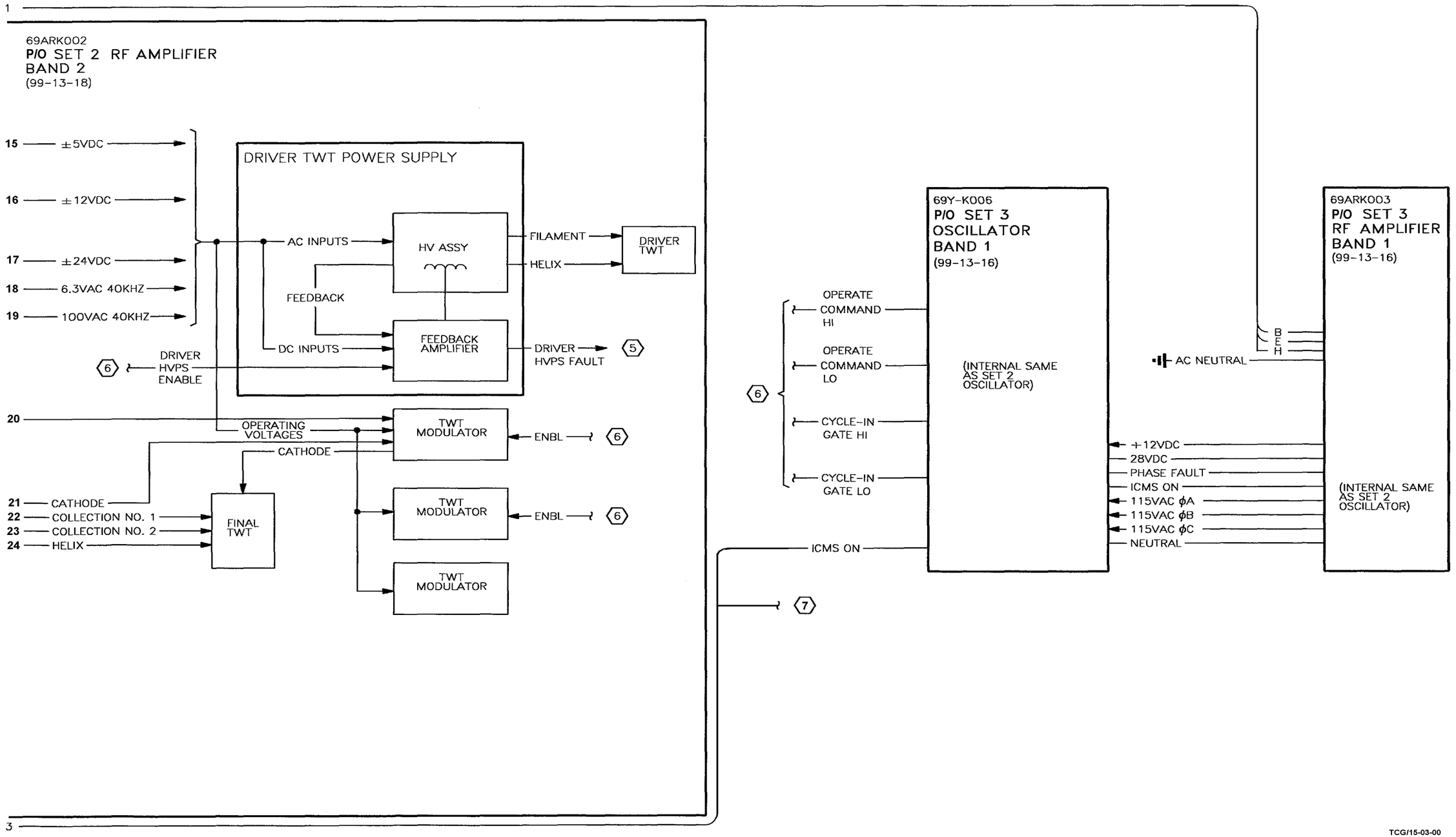

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Figure 13-4. ICMS Band 1 and 2 Power Distribution Simplified Schematic (Sheet 5)

LEGEND

1. SEE ICMS **BAND 1 & 2** POWER DISTRIBUTION SIMPLIFIED SCHEMATIC.
2. SEE ICMS **BAND 1 & 2** BIT SIMPLIFIED SCHEMATIC.
3. WEIGHT OFF WHEELS PROVIDES GROUND TO LOCK-OUT INHIBIT CIRCUIT.
4. REFER TO RWR POWER DISTRIBUTION SIMPLIFIED SCHEMATIC, SECTION II.
5. WHEN VALVE SOLENOID IS ENERGIZED, WITH ONE OR BOTH A/C ENGINES RUNNING, VALVE REDUCES AIRFLOW BY 90%.
6. SEE ICMS BAND 3 POWER AND CONTROL SIMPLIFIED SCHEMATIC.

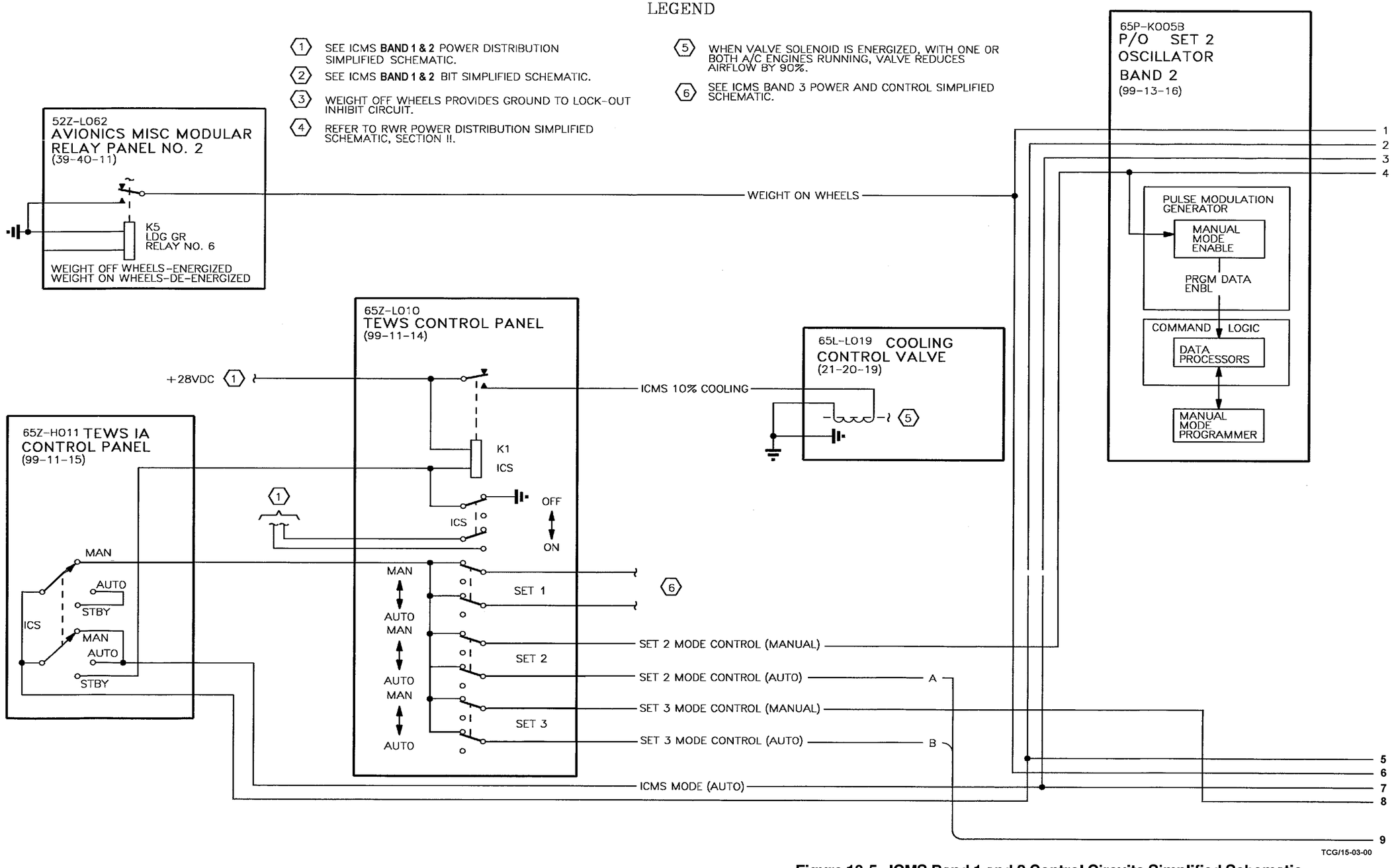

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Figure 13-5. ICMS Band 1 and 2 Control Circuits Simplified Schematic (Sheet 1 of 2)

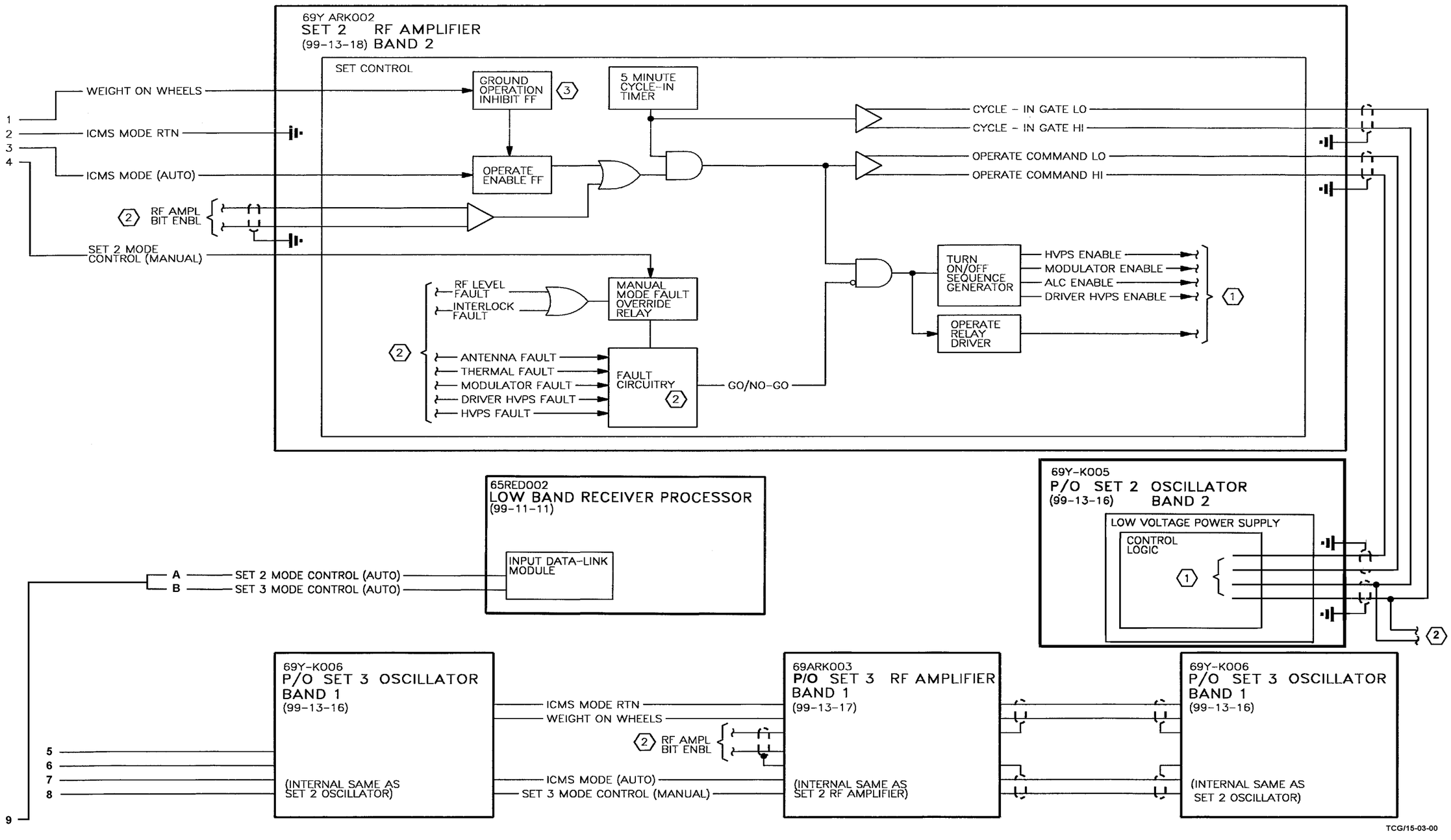

Figure 13-5. ICMS Band 1 and 2 Control Circuits Simplified Schematic (Sheet 2)

TO SR1F-15C-2-99GS-00-1

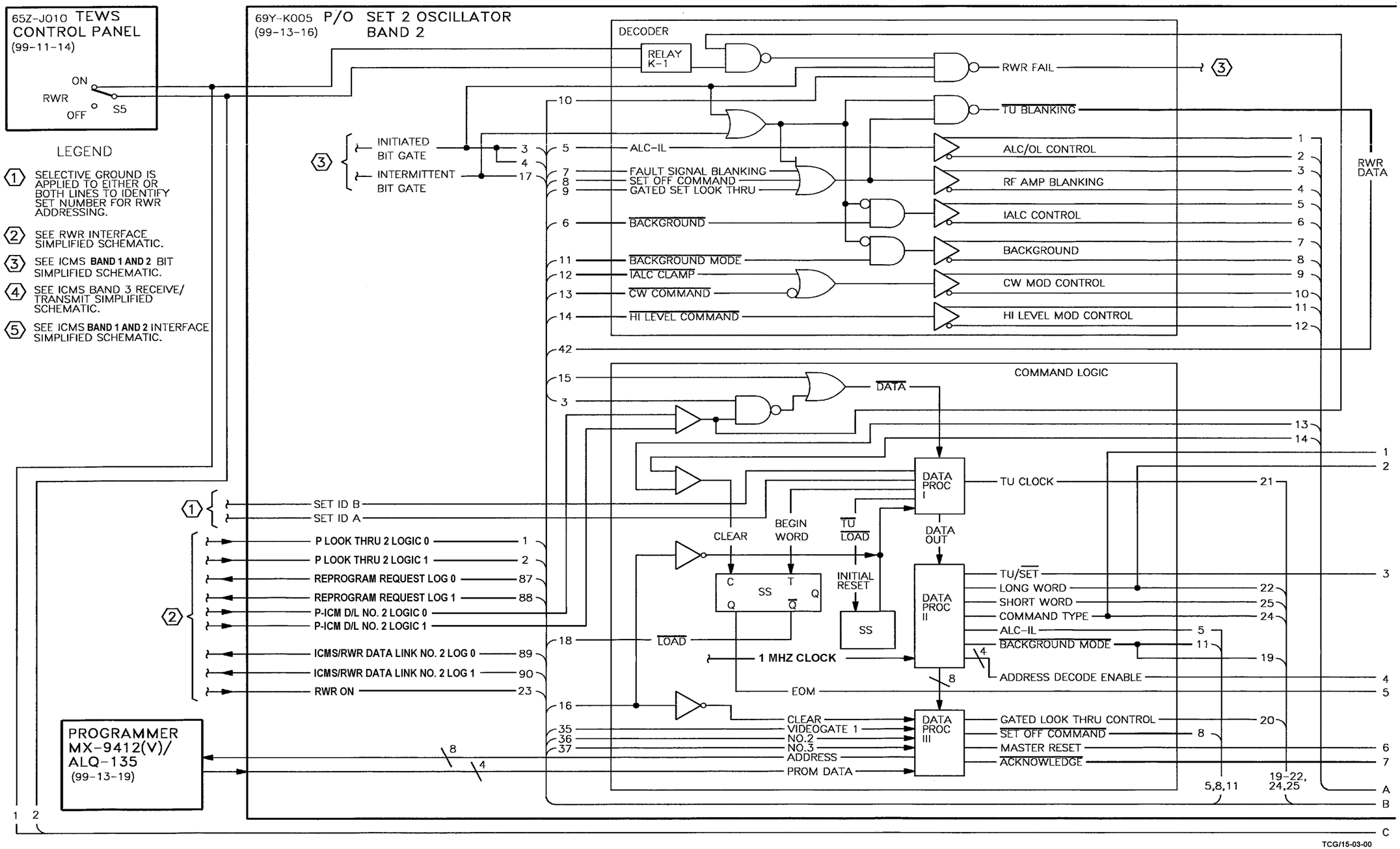

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 1 of 8)

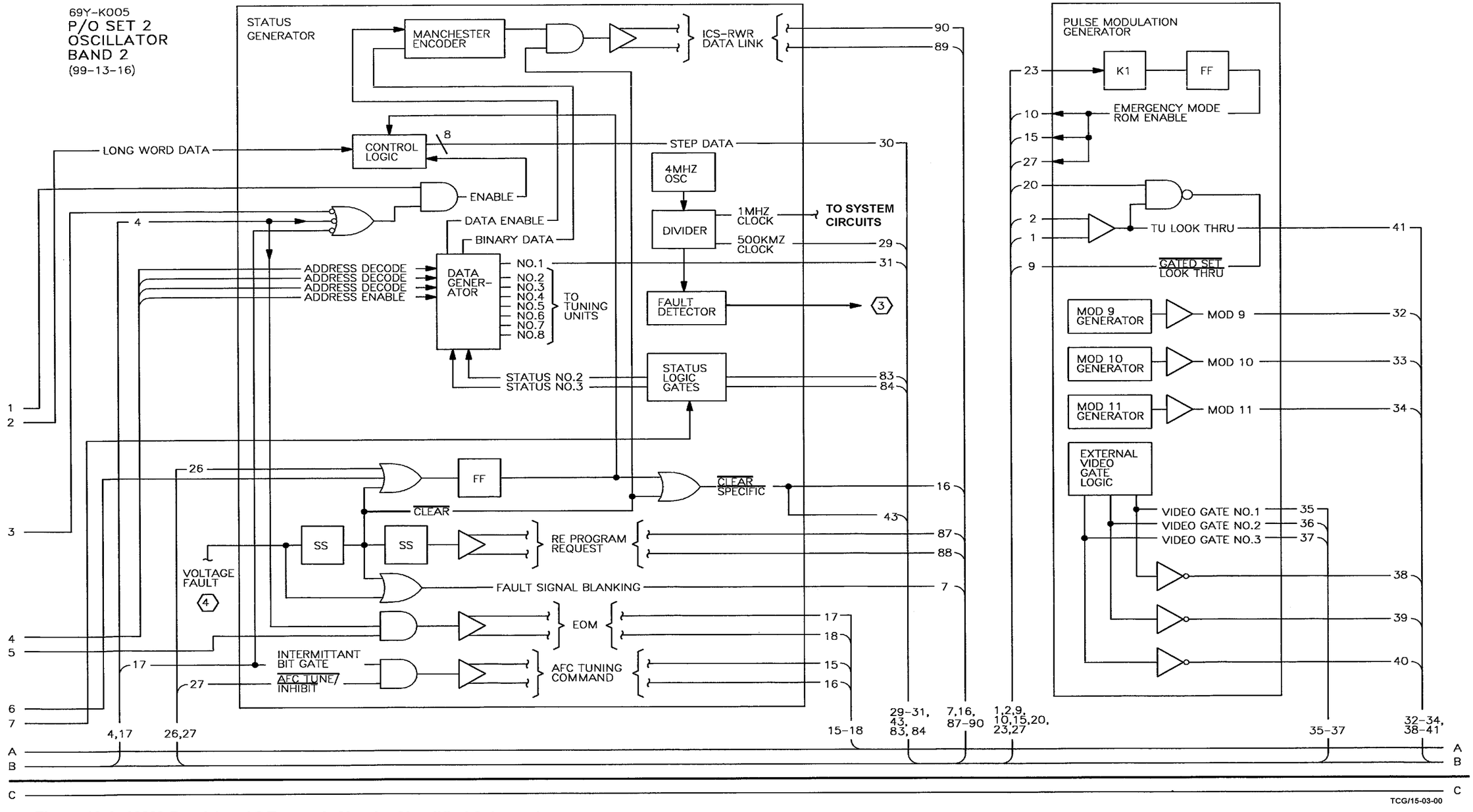

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 2)

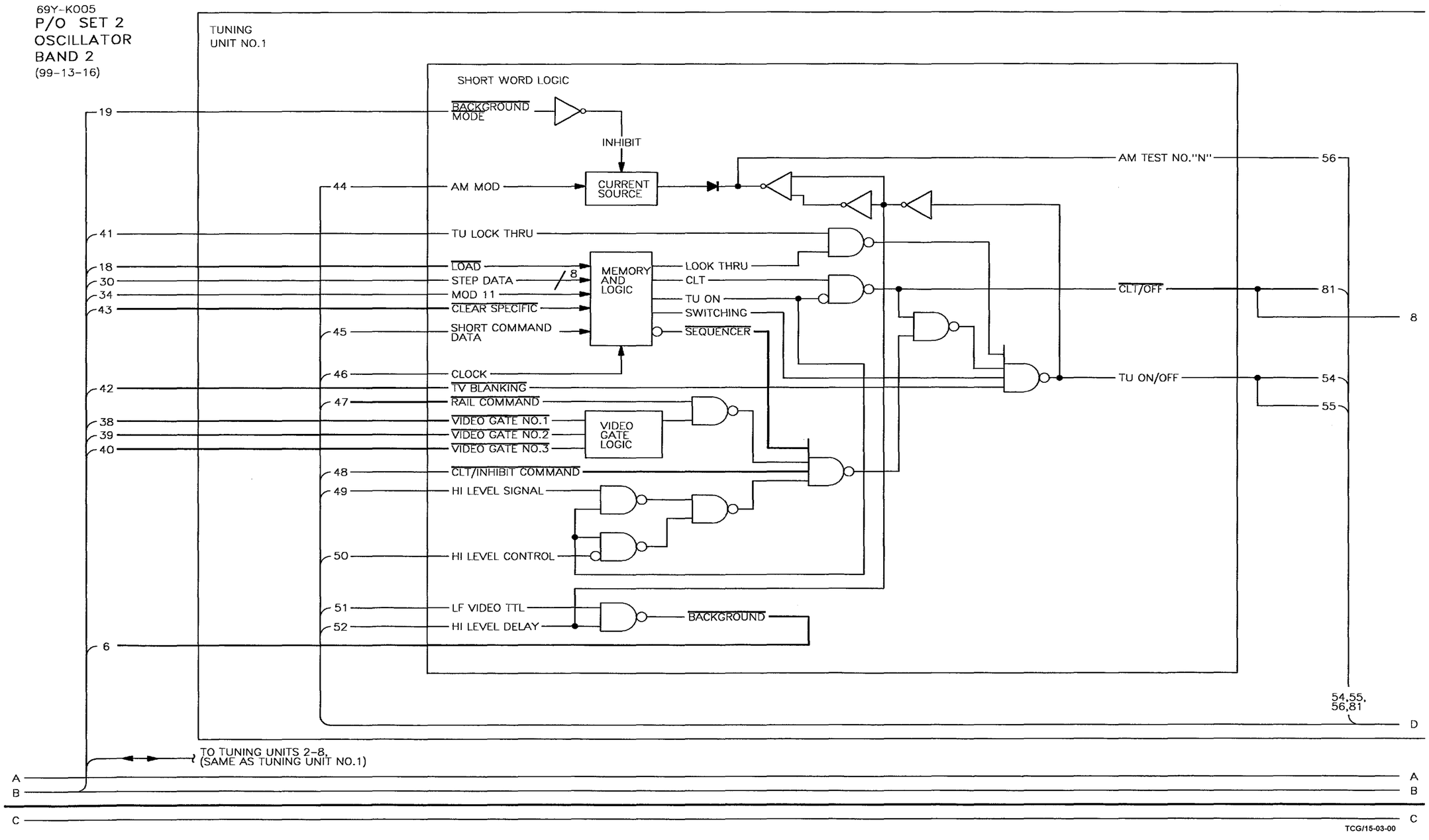

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 3)

69Y-K005
P/O SET 2 OSCILLATOR
BAND 2
(99-13-16)

TUNING UNIT NO.1

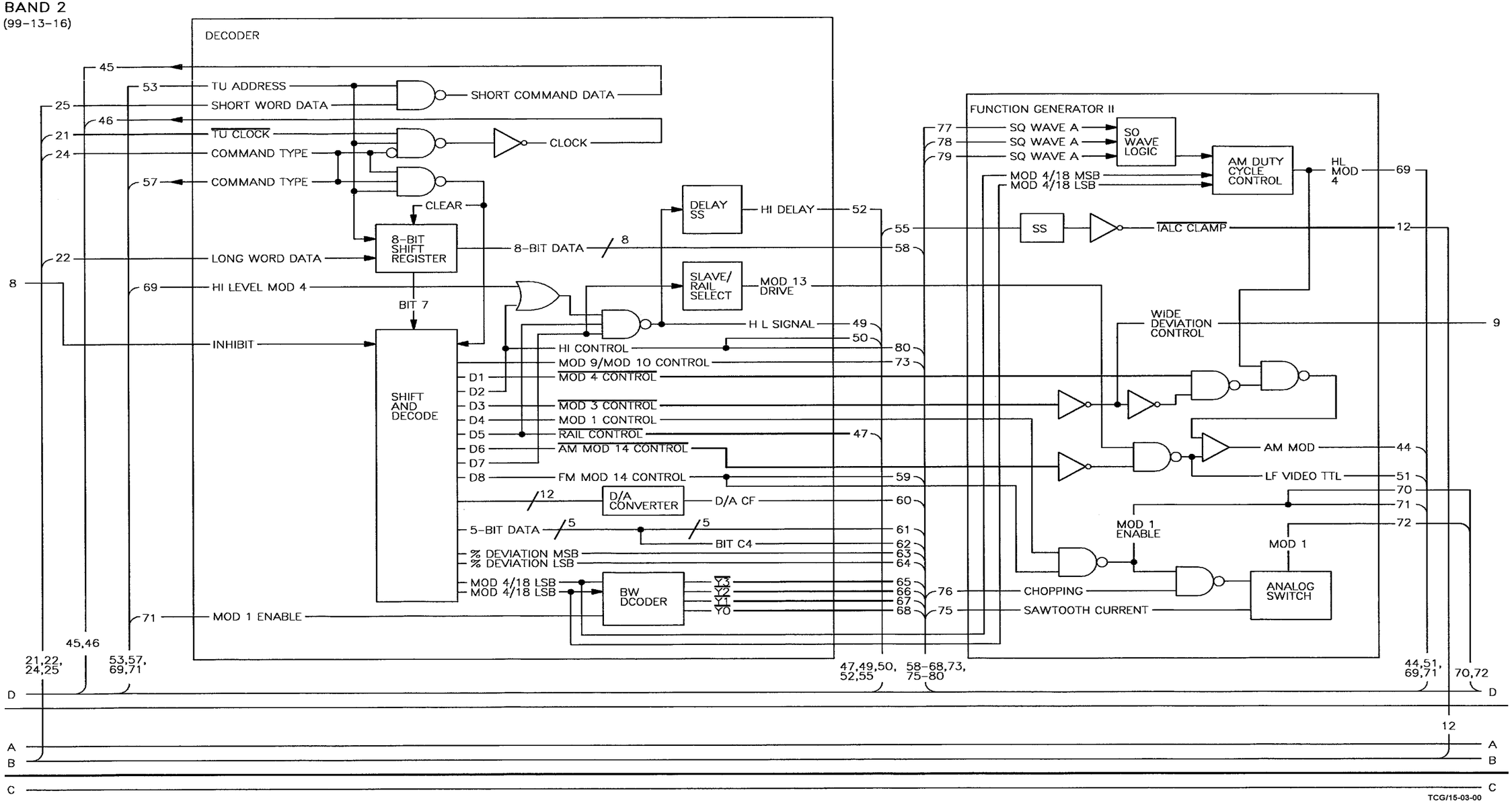

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 4)

69Y-K005
P/O SET 2 OSCILLATOR
BAND 2
(99-13-16)

TUNING UNIT NO.1

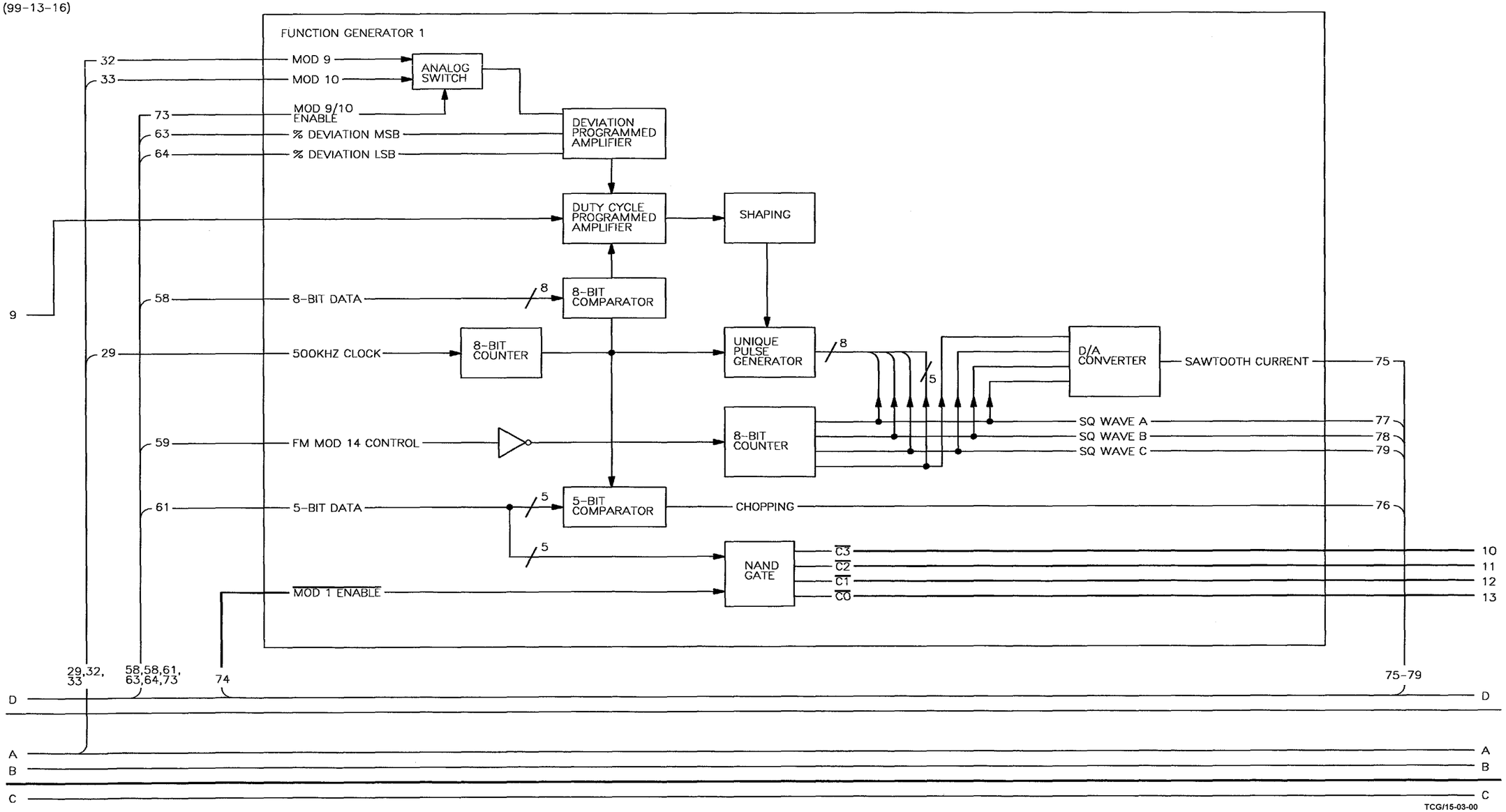

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 5)

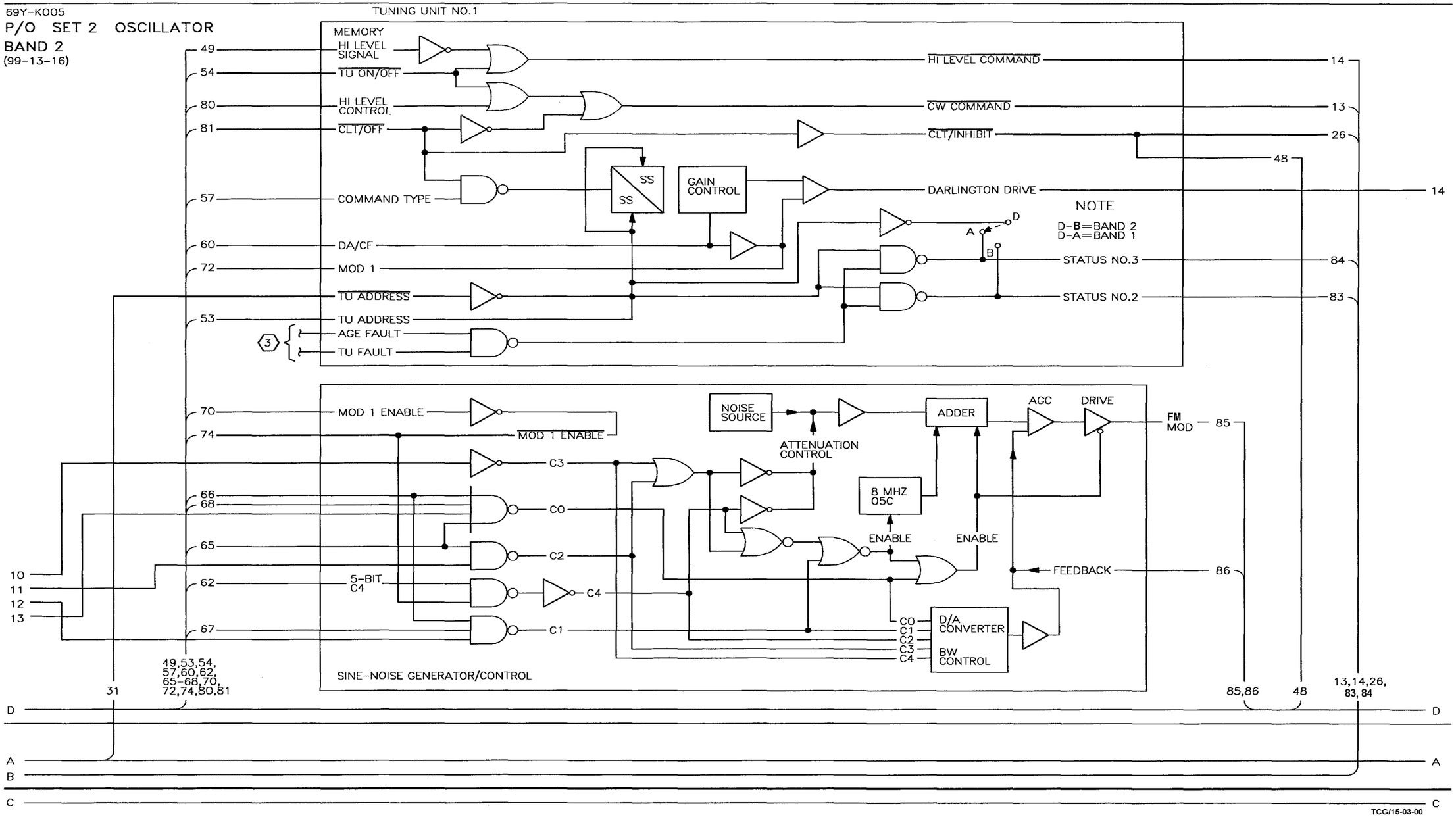

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 6)

TO SR1F-15C-2-99GS-00-1

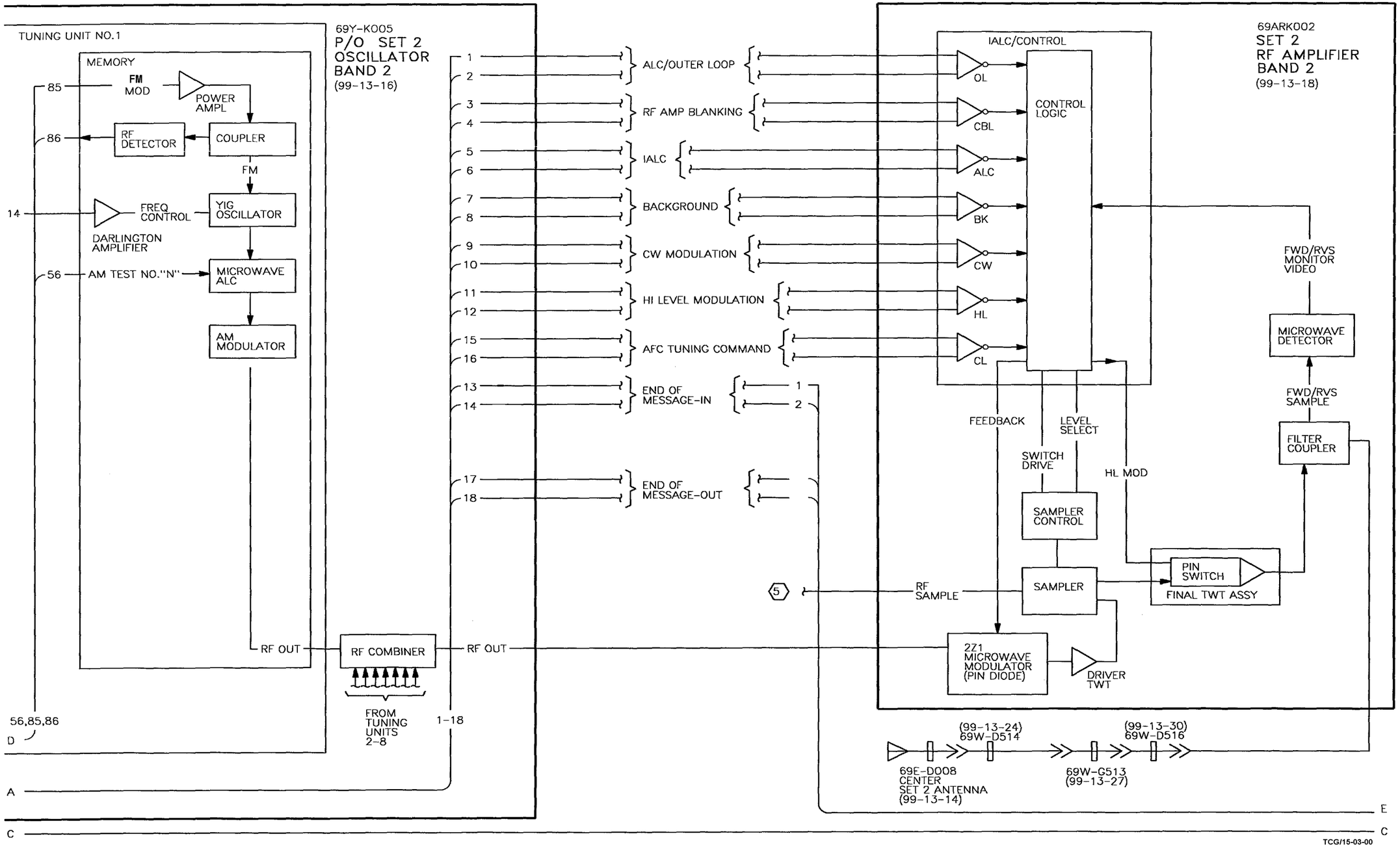

Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 7)

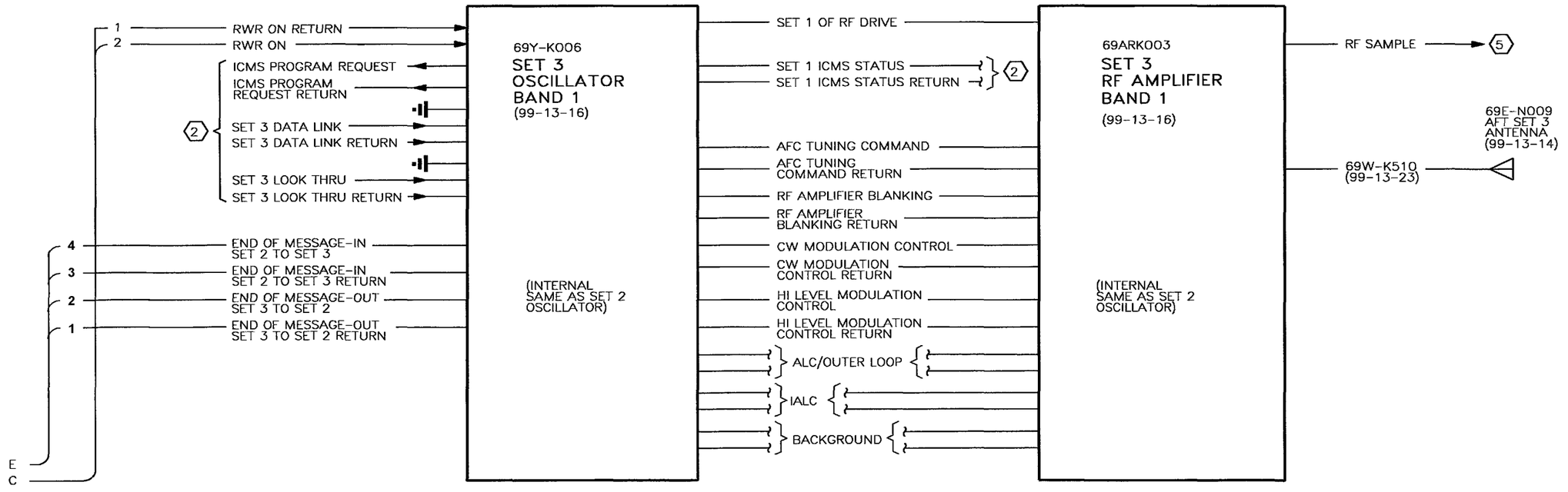

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Figure 13-6. ICMS Band 1 and 2 Transmit Circuits Simplified Schematic (Sheet 8)

LEGEND

(ORANGE)

FAILED POSITION SHOWN

1. CRITICAL UNITS WITHIN THE RF AMPLIFIER HAVE AN INTERLOCK FEATURE, ABSENCE OF ANY OF THESE ASSEMBLIES WILL CAUSE AN INTERLOCK FAULT.
2. +28VDC APPLIED WITH LIGHTS TEST SWITCH ON.
3. SEE ICMS **BAND 1 AND 2** CONTROL SIMPLIFIED SCHEMATIC.
4. SEE ICMS **BAND 1 AND 2** POWER DISTRIBUTION SIMPLIFIED SCHEMATIC.
5. SEE ICMS **BAND 1 AND 2** TRANSMIT SIMPLIFIED SCHEMATIC.
6. **SEE BAND 3 BIT SIMPLIFIED SCHEMATIC.**

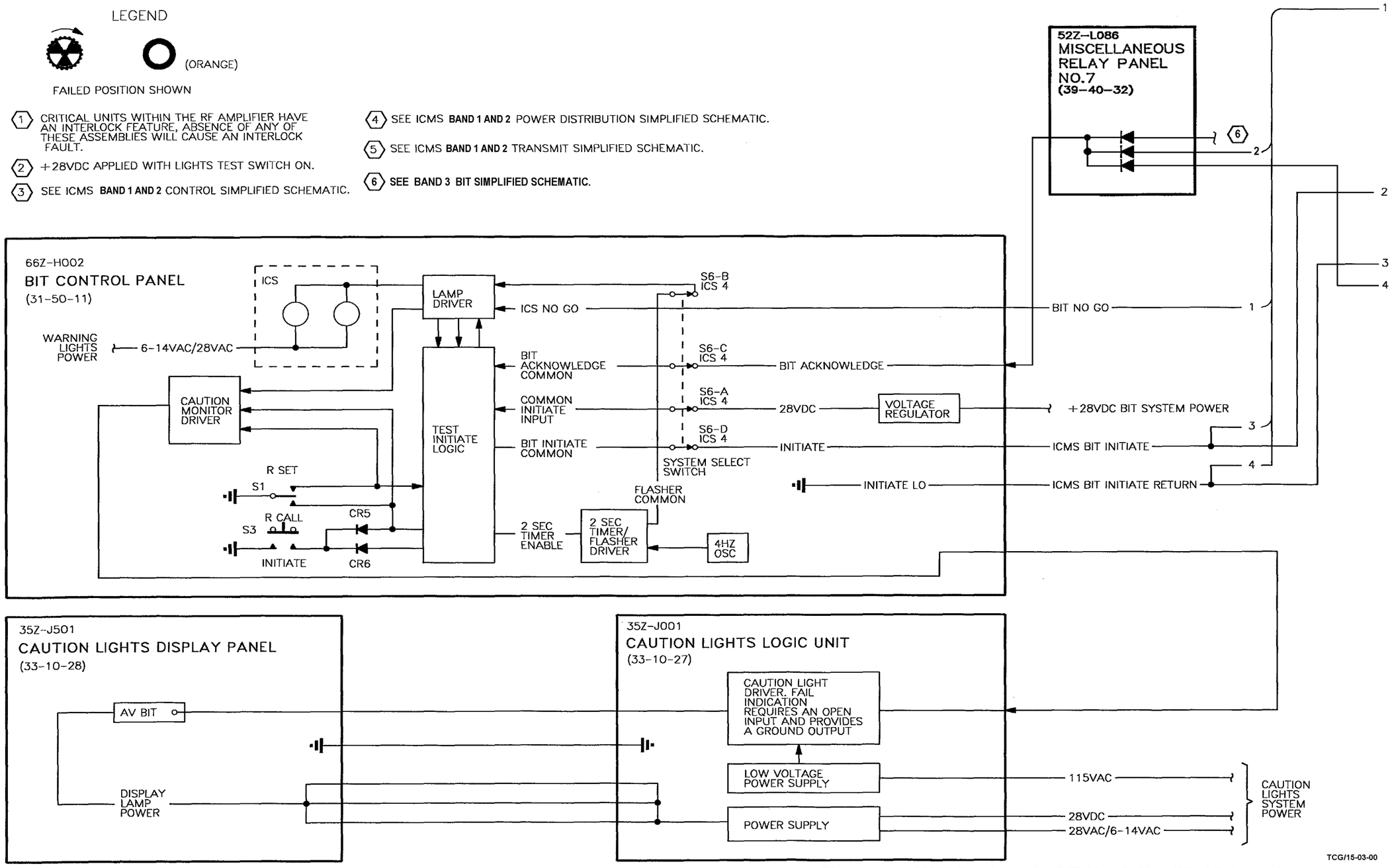

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 1 of 8)

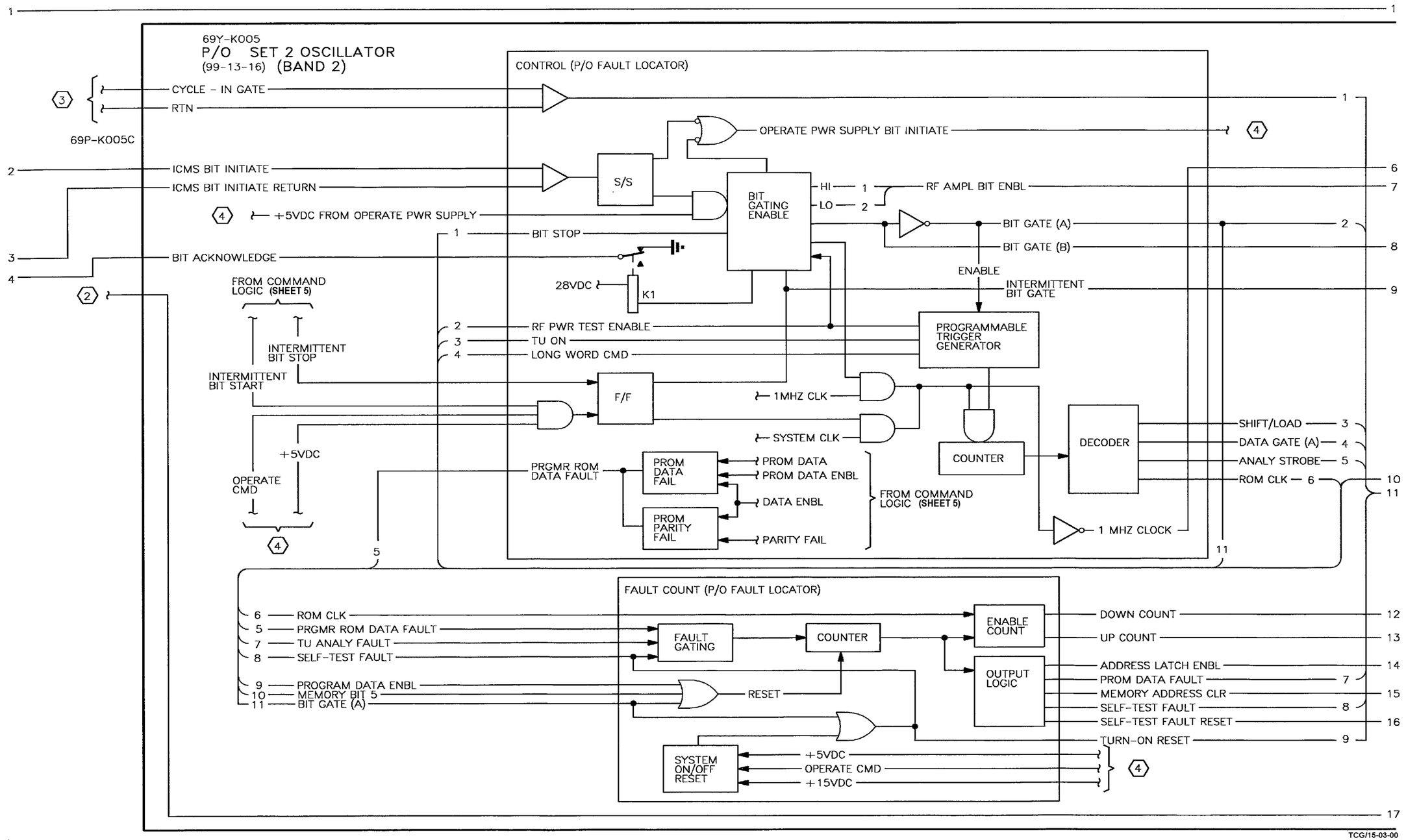

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 2)

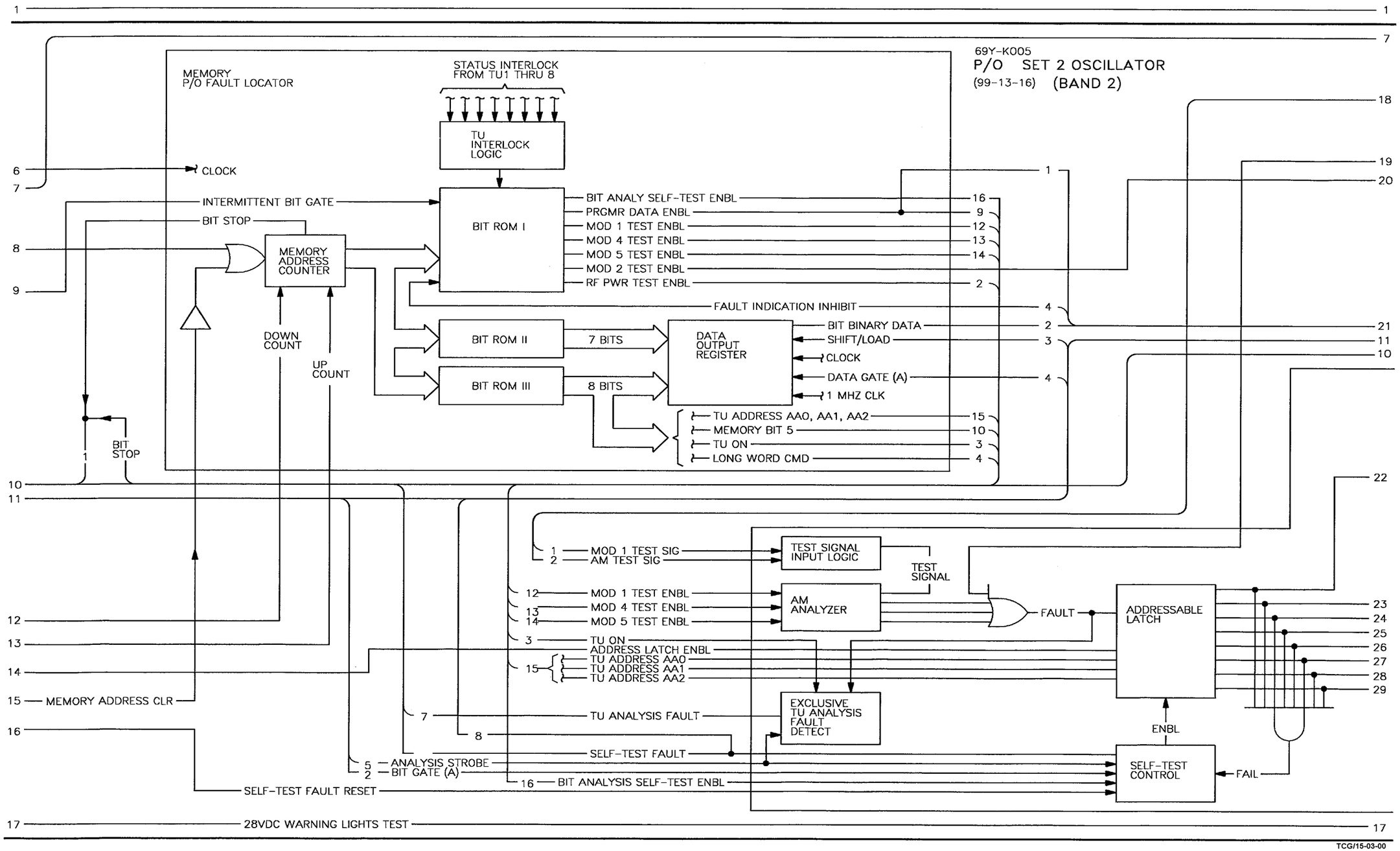

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 3)

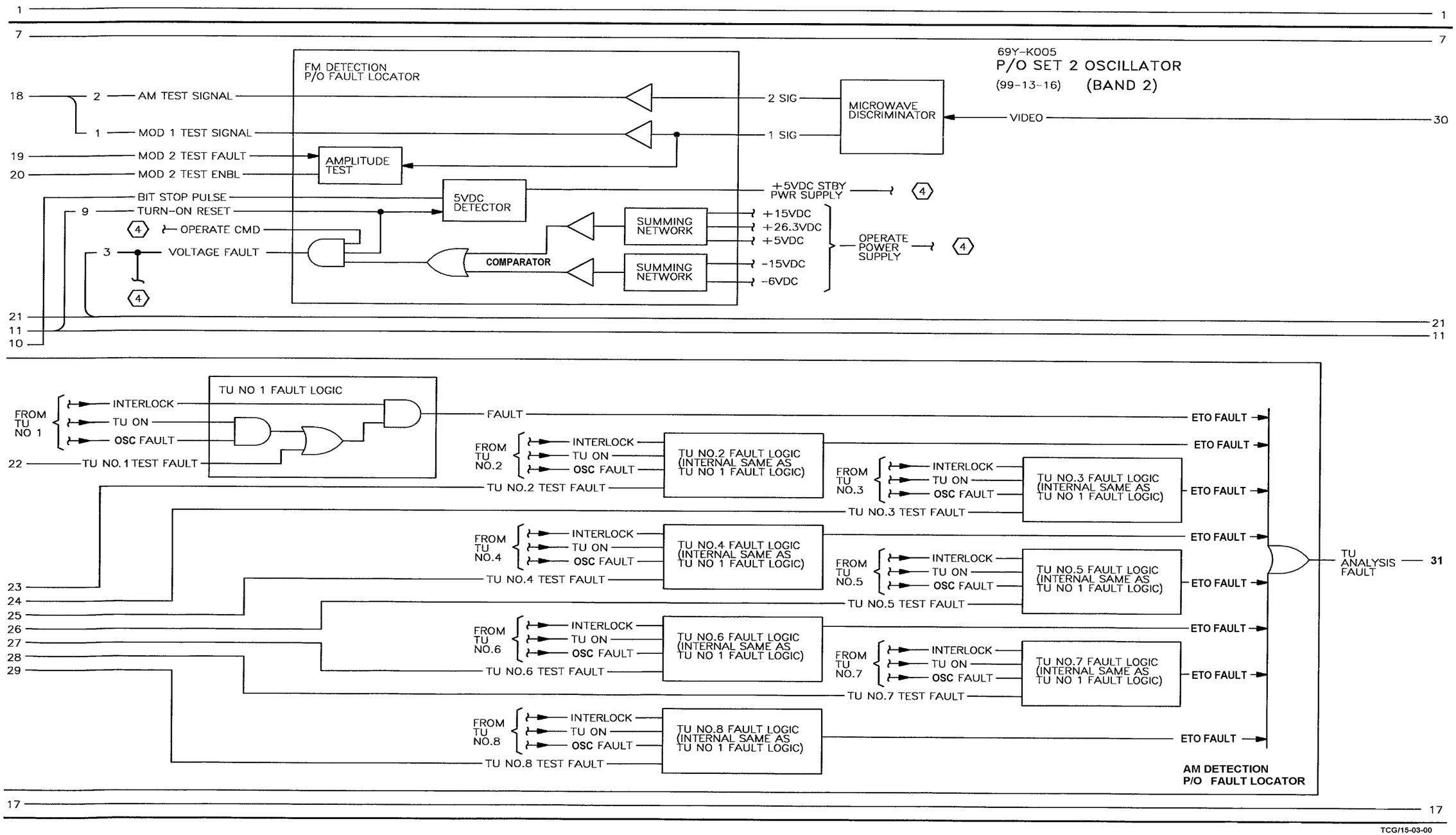

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 4)

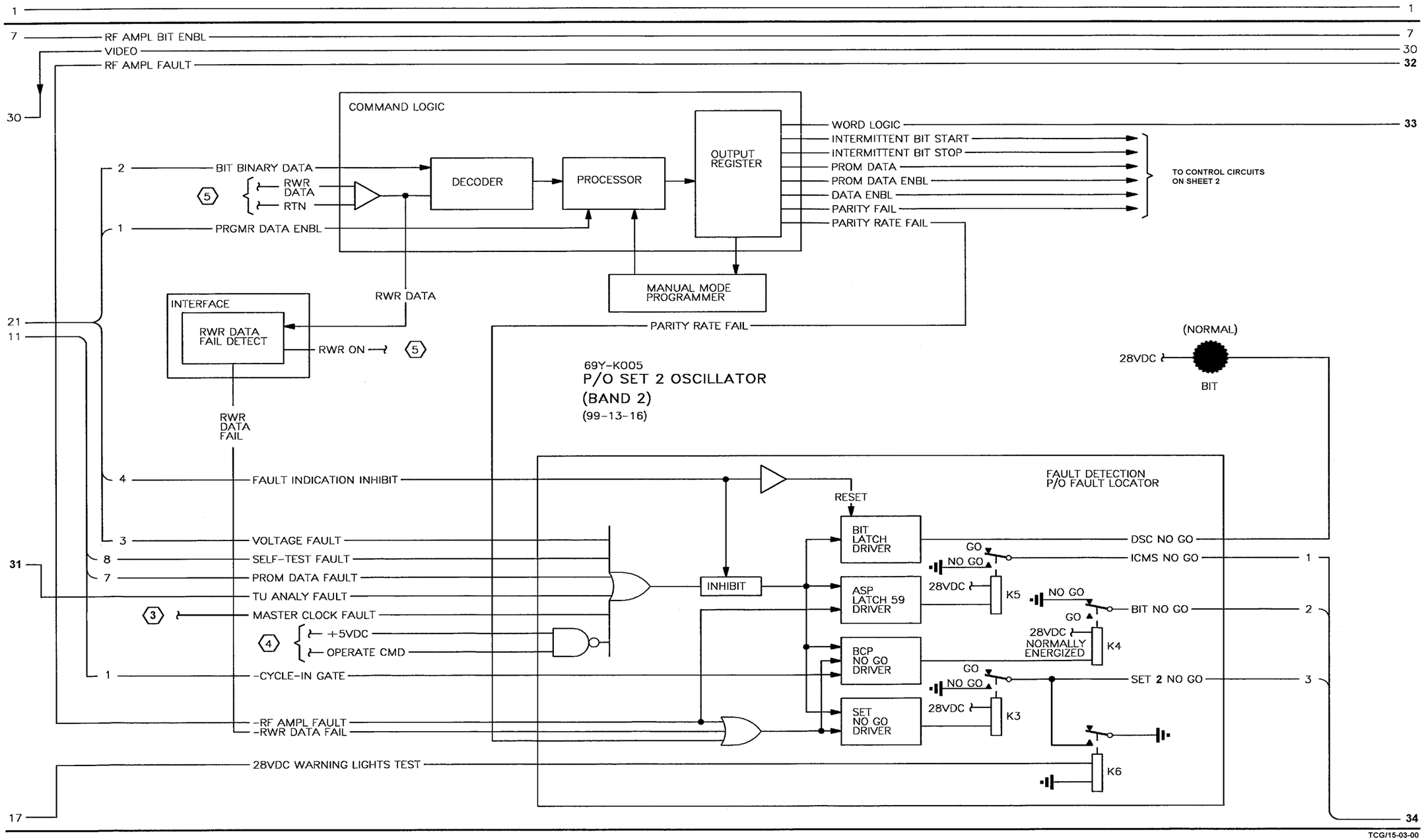

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 5)

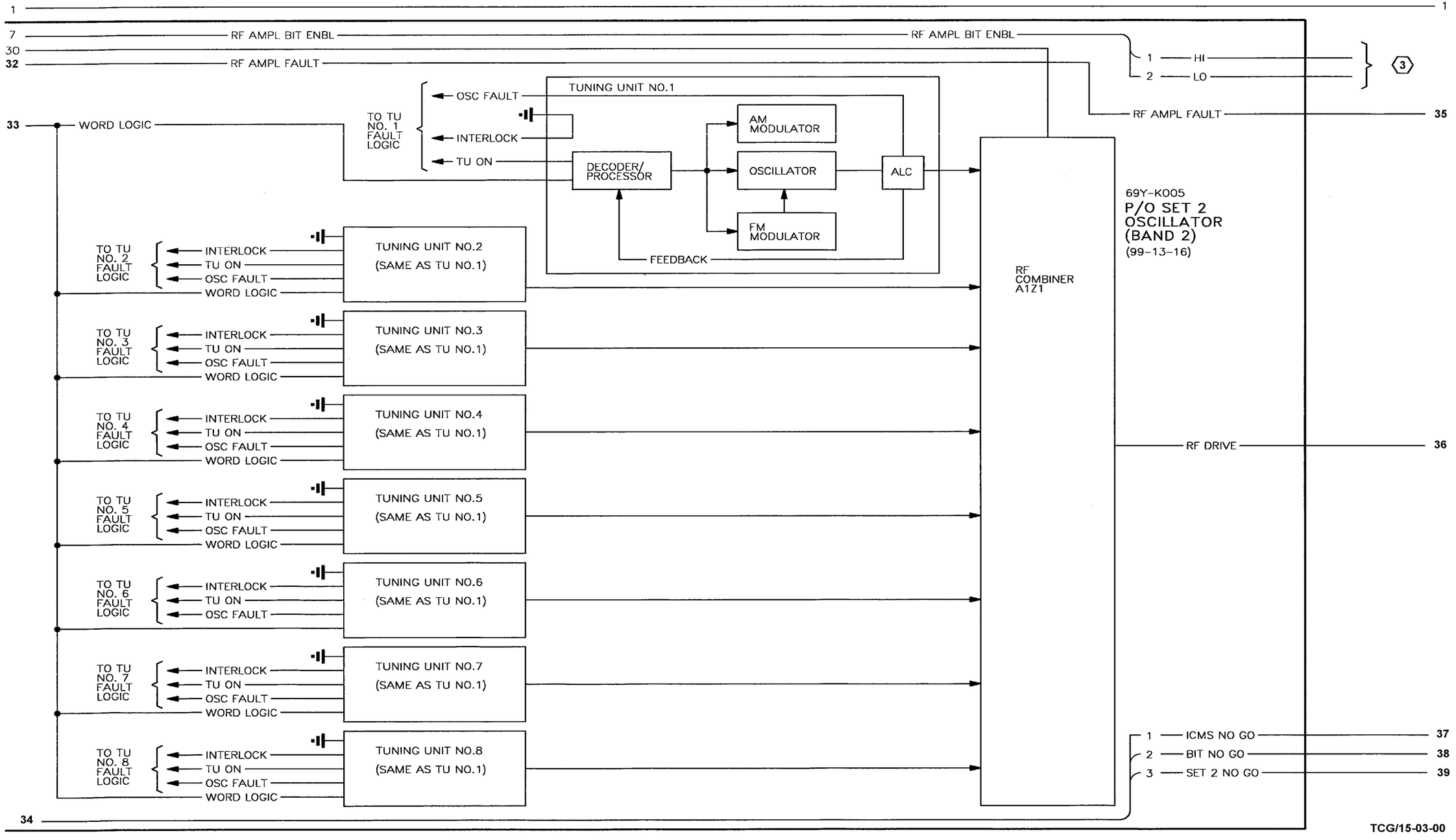

Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 6)

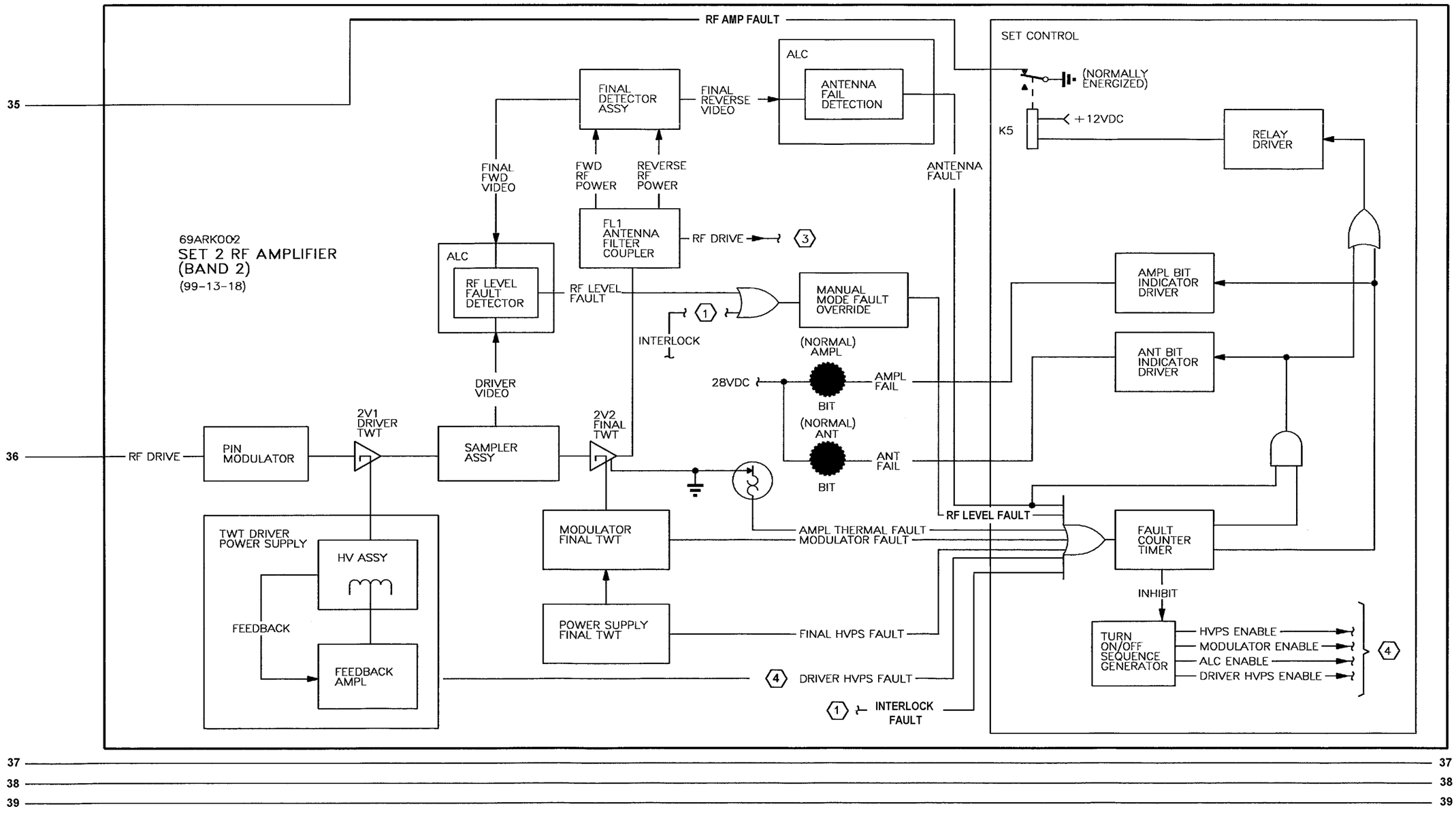

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Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 7)

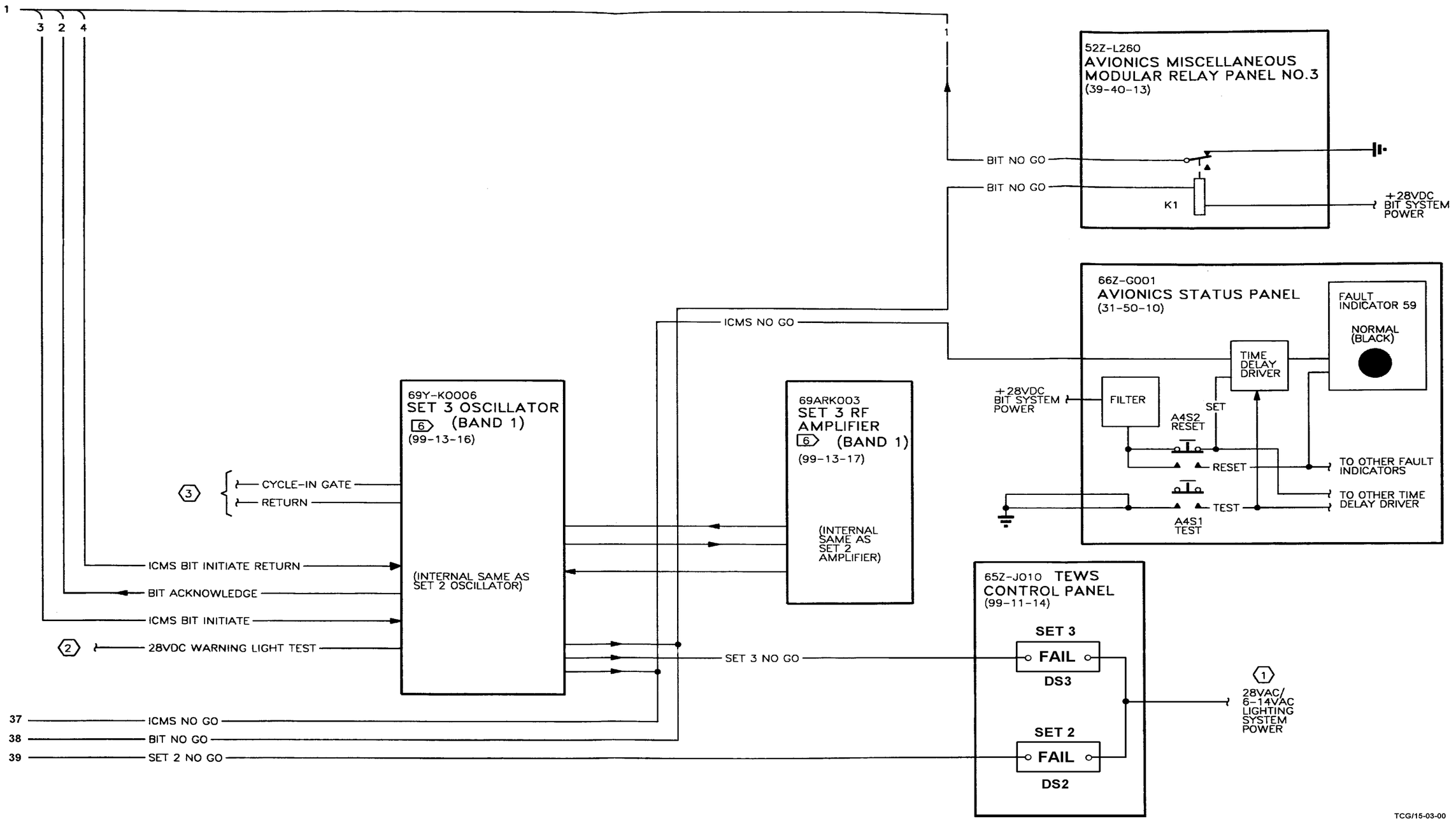
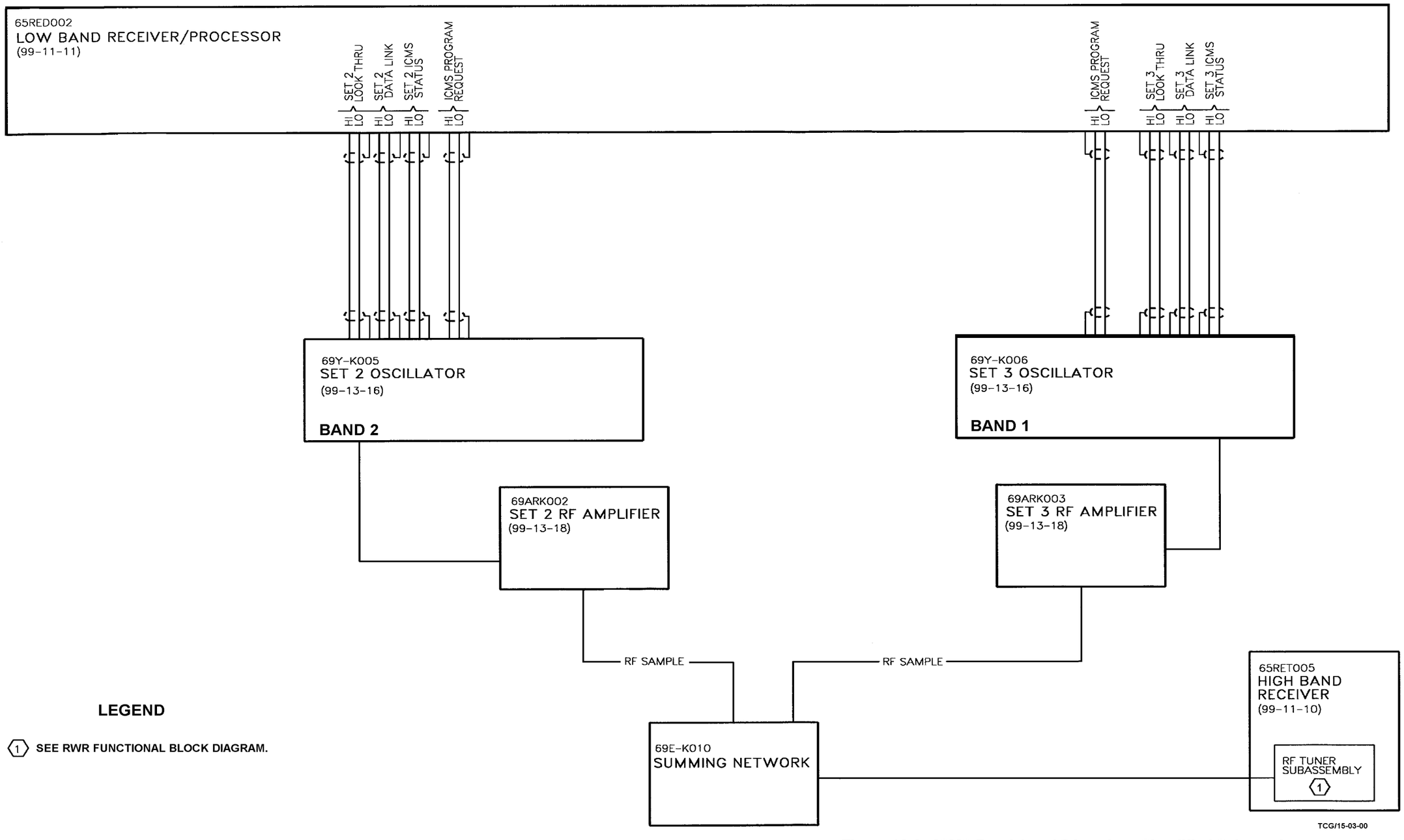


Figure 13-7. ICMS Band 1 and 2 BIT Circuit Simplified Schematic (Sheet 8)



LEGEND

1 **SEE RWR FUNCTIONAL BLOCK DIAGRAM.**

Figure 13-8. ICMS Band 1 and 2 Interface Simplified Schematic

Manual mode, an emergency mode, is meant to be used during RWR failure and overrides RF power failure monitoring in the RF Amplifier and prevents system shutdown.

13-47. With the ICS switch on the TEWS IA control panel in the MAN position, ICS relay K1 in the TEWS control panel is deenergized, and 100% ECS cooling air is supplied to the ICMS system. The ICMS MODE RTN signal is applied to the SET-2 and SET-3 switches in the TEWS control panel. The ICMS MODE (AUTO) signal is routed through the oscillator to the RF Amplifier set control module. ICMS MODE (AUTO) signal applied to the set control module starts the OPERATE COMMAND and also enables the turn on/off sequence generator and operate relay driver if no failures exist. The ICMS enable is inhibited if the ground operation inhibit circuit is active or the 5 minute cycle-in timer has not timed out. The ground operation inhibit circuit is active when a WEIGHT ON WHEELS signal is available. The WEIGHT ON WHEELS signal is an open circuit made by contacts of LDG GR RELAY NO. 6 being deenergized by the LMLG WOW switch. The open circuit resets a flip-flop located in the IALC/control module in the RF Amplifier and inhibits normal operation.

13-48. The OPERATE COMMAND produced by the set control module is sent to the oscillator low voltage power supply control logic module to enable the operate power supply in the oscillator. The turn on/off sequence generator sequentially enables the driver TWT power supply, final TWT power, modulator, and automatic level control within the RF Amplifier. The operate relay driver energizes operate relay 2A1K2 applying primary power to the final TWT power supply. See Figure 13-4.

13-49. Setting the SET-2 or SET-3 MAN/AUTO switch on the TEWS control panel to MAN applies the ICMS MODE RTN signal (ground) to the MODE CONTROL (MANUAL) signal input to the Oscillator, RF Amplifier, and RWR Low Band Receiver/ Processor. With manual mode selected, the oscillator manual mode enable circuit on the pulse modulation generator provides a PRGM DATA ENBL signal to the data processors on the command logic module enabling the program stored in the manual mode programmer. The RF Amplifier manual mode fault override circuit on the set control module inhibits the RF LEVEL FAULT and circuit INTERLOCK FAULT preventing system shutdown. If manual mode was selected because the system failed in auto mode and the RF LEVEL FAULT and circuit INTERLOCK FAULT caused this failure, putting the system in manual mode enables the turn on/off sequence generator, and turns off the ICS light on the BIT control panel and the SET-2 FAIL or SET-3 FAIL light on the TEWS control panel. See Figure 13-7. Fail indicator 59 on the ASP and the AMPL BIT indicator on the RF Amplifier remain set because of the failure occurring during auto mode. The low band receiver/processor input data link module tells the RWR that the ICMS is in manual mode and is using the program stored in the manual mode programmer and no longer needs RWR data inputs.

13-50. Auto Mode. Auto mode is selected by putting the MAN/AUTO/STBY switch on the TEWS IA control panel to AUTO. The same circuits are enabled as in manual mode except the ICMS MODE RTN is no longer applied to the MODE CONTROL (AUTO) input to the Oscillator and RF Amplifier. The manual mode fault override circuit on the RF Amplifier set contol module becomes inactive, and the RF LEVEL FAULT and circuit INTERLOCK FAULT are gated to the fault circuitry if a failure occurs. In the oscillator, the PRGM DATA ENBL signal produced by the manual mode enable circuit on the pulse modulation generator becomes inactive and the MODE CONTROL (AUTO) input to the RWR low band receiver/processor input data link module is open, indicating to the RWR that the ICMS is in auto mode and ready to receive data command inputs from the RWR.

13-51. **Transmitting Circuits.** See Figure 13-6. The data link signals from the RWR system are sent to the oscillator input/output section of Sets 2 and 3. The set not processing a previous data word receives the new data, does a parity check and produces a response to the RWR acknowledging receipt of the data. Operation of the two sets is identical so only Set 2 operation is described.

13-52. Data coming in is Manchester decoded by command logic module. The decoded data is sent to the first of three LSI data processors. Data processor I compares set ID coding with the set identification bits part of the data word. If the comparison matches, the data word is sent to data processor II for more analysis. Long word and short word data are extracted from the data word and are sent to tuning units to develop modulator command data. The long word data is also

sent to status generator module to produce step data for tuning the yig oscillators in the tuning units. When an EMERGENCY MODE ROM ENABLE is produced by selection of ICS MAN, the RWR data link words are inhibited and data processor III addresses the programmer ROM for tuning and modulation data. An END OF MESSAGE command received from Set 2 means the data word has been received and produces a CLEAR command to delete the word data from the Set 3 data processors.

13-53. After data loading has been done, an acknowledge signal is produced by the status generator and is Manchester encoded and sent to the RWR by way of the ICS DATA LINK lines. This completes the communication loop cycle between the RWR and ICMS systems. The step data and modulation information is sent to the eight tuning units, one of which produces an RF output signal containing the commanded characteristics. Operation of the eight tuning units is identical and only TU no. 1 operation is described.

13-54. Short word data is sent from the input/output section to the decoder module. If the tuner address agrees, the data is sent to the short word logic module to be decoded into am modulation control commands. Function generators I and II operate under the control of the decoder module to produce and process the amplitude modulation signals that are to be sent to the yig oscillator module. The sine-noise generator/control module produces FM modulation information that is also passed to the yig oscillator module. Step tuning data, decoded by a D/A converter in the decoder module, is sent to the memory module and processed to produce an analog voltage proportional to the commanded oscillator center frequency. The analog voltage is then sent to a Darlington Amplifier to develop a proportional current signal that drives the yig oscillator to its commanded frequency.

13-55. The RF output of the yig oscillator is modulated and level-controlled by the microwave level control/ modulator module and is sent to an RF combiner to be joined with the RF outputs of tuning units 2 through 8.

13-56. A programmed Set 2 LOOK THROUGH COMMAND from the RWR is sent to the pulse modulate generator and then to the addressed tuning unit short word logic module. This produces a tuning unit OFF command which inhibits RF output for the time of the command. This enables the RWR to look at the covered frequency range to determine if more jamming is required. A command is also sent to the RF Amplifier to blank its output. RF Amplifier blanking also occurs if a fail signal is produced by the fault detection unit.

13-57. The RF output from the combiner is sent to Set 2 RF Amplifier PIN DIODE modulator. CW and high level modulation commands are sent to the RF Amplifier Automatic Level Control Logic circuits, then applied to the PIN DIODE modulator to AM modulate the RF signal. The modulated RF is sent to the driver TWT for amplification. The output of the Driver TWT is monitored by the Automatic Level Control circuit for leveling, and then coupled to the Final TWT for final amplification. Final TWT output is then sent to the Set 2 antenna through a directional coupler.

13-58. **BIT Circuits.** See Figure 13-7 and Table 13-7. Built-in test of the ICMS is separated into three categories: continuous BIT, initiated BIT and intermittent BIT. The BIT function of Set 2 is used for description as Set 3 BIT functions are identical.

13-59. Continuous BIT. The continuous BIT circuitry continuously and automatically monitors specific system parameters in the oscillator and RF Amplifier when the system is in manual or auto mode.

13-60. Continuous BIT circuits in the Oscillator continually monitor operating voltages, current, phase, temperature, circuit interlock, master clock status, RWR to ICMS data line, RWR data parity rate, and tuning unit RF output. Operating voltages are monitored by a weighted summing network on the FM Detection module. Voltage deviations are detected by this sensing network and a VOLTAGE FAULT is sent to the Control Logic module to disable the operate power supply and also to the Fault Detection module to enable BIT fail indications. All standby voltages are tested by this sensing network because all operating voltages are missing if any standby voltage is missing and a VOLTAGE FAULT is produced. PHASE FAULT, OPERATE FAULT, THERMAL FAULT, and INTERLOCK FAULT also cause a VOLTAGE FAULT because of the lack of operating voltages at the sensing network. A phase detector in the low voltage power supply (see Figure 13-4) senses the three phase input and sends a PHASE FAULT to the Control Logic module to deenergize relay A3A1K1 if there is a failure. Deenergized relay A3A1K1 applies ground to the operate switch drive, disabling the operate power supply. OPERATE FAULTS are failures sensed in the operate power supply and applied to the Control Logic

module to disable the operate power supply and enable BIT fail indications. A normally open thermal switch (see Figure 13-4) on a critical part of the low voltage power supply frame sends a THERMAL FAULT to the operate switch drive, disabling the operate power supply and enabling BIT fail indications when the temperature exceeds 175°F ± 5°F. Critical units in the Oscillator have a circuit interlock. Lack of any of these assemblies causes an INTERLOCK FAULT, disabling the operate power supply and enabling BIT fail indicators. A STANDBY FAULT is a current failure sensed in the standby power supply and at the output of the base drive. A STANDBY FAULT (see Figure 13-4) shuts down both the standby and operate power supplies, disabling the ICMS. The ICS light on the BCP lights indicating system failure. Master clock status is monitored by the 1 MHz clock fault detection circuit on the status generator. A MASTER CLOCK FAULT is applied to the fault detection module to enable BIT fail indications. The RWR to ICMS data line is continuously monitored when the system is in auto mode. An RWR ON signal is applied to the RWR fail detection circuit on the interface module. RWR DATA is applied to the command logic module. RWR DATA is applied to the command logic module and to the RWR fail detection circuit. When the RWR ON signal is available, and no RWR DATA is available, an RWR DATA FAIL is produced and applied to the fault detection module to enable BIT fail indications. Also, RWR data parity rate is monitored by the data processors on the command logic module and a PARITY RATE FAIL is applied to the fault detection module to enable BIT fail indications. Each tuning unit RF output is monitored on each individual tuning unit by the ALC circuit within the tuning unit. If the output of the tuning unit drops below a level that can be corrected by the ALC circuit, an ETO FAULT is produced. The ETO FAULT is applied to the respective TU no. 1 through TU no. 8 fault logic circuit on the AM detection module and gated to the fault detection module as a TU ANALY FAULT to enable BIT fail indications if the TU ON signal is available and if circuit interlock exists.

13-61. Continuous BIT circuits in the RF Amplifier continually monitor forward and reverse power, the driver TWT power supply, final TWT power supply, final TWT overtemperature, low voltage power supply, circuit interlock, and the final TWT modulator. Forward power delivered to the antenna is monitored by the RF level fault detector circuit on the ALC module. A threshold is set so a fault is produced if power drops below rated output. An RF LEVEL FAULT is gated through the manual mode fault override circuit to the set control module to enable BIT fail indications. When the system is in manual mode, the RF LEVEL FAULT is inhibited, allowing system operation at a reduced power output. Reflected power from the antenna transmission line is monitored by the antenna fail detection circuit, also on the ALC module.

Table 13-7. BIT Operating Modes

ICMS Mode	Continous	Initiated	Intermittent
Standby (Wheels down and weight on wheels)	Continuous after ICMS is operational	BCP initiates. (Two 20 usec pulses radiated)	
Standby (Wheels up)	Continuous after ICMS is operational	BCP initiates. (Two 1.5 sec pulses radiated)	
Operate (AUTO) (Wheels down and weight on wheels)	Continuous	BCP initiates. (Two 20 usec pulses radiated)	

Table 13-7. BIT Operating Modes

ICMS Mode	Continous	Initiated	Intermittent
Operate (Wheels up)	Continuous		Started by RWR and may be stopped before test completion. Test identical to initiated BIT, except no RF power output test.

If a VSWR threshold is exceeded the ANTENNA FAULT is produced and is applied to the set control module to enable BIT fail indications. Both the driver TWT power supply and the final TWT power supply are continuously monitored for overvoltage and overcurrent conditions. Both supplies send fault signals, the DRIVER HVPS FAULT and FINAL HVPS FAULT, to the set control module to enable BIT fail indications. A normally closed thermal switch attached and grounded to the final TWT sends a THERMAL FAULT to the set control module enabling BIT fail indications when the temperature exceeds 180° C ± 5°C. The low voltage power supply is continuously monitored for overvoltage and overcurrent conditions and automatically shuts down should either condition exist. Relay K5 on the set control module deenergizes because of the lack of 12VDC at the coil, causing an RF AMPL FAULT to the Oscillator. The AMPL BIT indicator on the RF Amplifier sets because of the lack of bias voltage at the driver. Critical units in the RF Amplifier have an interlock. Lack of any of these assemblies causes an INTERLOCK FAULT to the set control module to enable BIT fail indications. The INTERLOCK FAULT is also gated through the manual mode override circuit and is inhibited when the system is in manual mode. The final TWT modulator produces a fault signal to the set control module to enable BIT fail indicators when there is a loss of the internal sustaining modulation circuits, the duty cycle or pulse width is out of tolerance and the PRF is in excess of established limits.

13-62. Initiated BIT. Initiated BIT can be done with the ICMS in the standby or operate (AUTO) modes using the BCP. The time of the initiated BIT period is approximately 17 seconds and is enabled by pressing and releasing the INITIATE switch on the BCP when the system select switch is in the ICS position. Initiated BIT is a read only memory (ROM) controlled test sequence made up of a BIT analysis and a test of the RF Amplifier.

13-63. Pressing and releasing the INITIATE switch applies a BIT INITIATE signal to the oscillator fault locator control module. The control module sends an OPERATE PWR SUPPLY BIT INITIATE signal to the low voltage power supply (LVPS) (see Figure 13-4) to enable operate voltages. The LVPS must respond within a specified time frame or initiated BIT will not occur. The LVPS response is monitored by way of the 5VDC input. When the 5VDC becomes active the initiated BIT cycle is enabled and the operate power supply is held on. Also, control relay K1 is held energized telling the BCP that the BIT program is in progress, BIT GATE (B) enables the memory address counter, BIT GATE (A) enables the programmable trigger generator, and the 1 MHZ CLK signal is gated to the counter.

13-64. The programmable trigger generator produces three different pulse repetition rates determined by the RF PWR TEST ENABLE, TU ON, and the LONG WORD CMD inputs. The counter output is decoded to enable the DATA GATE (A), SHIFT/LOAD, ANALY STROBE, and ROM CLK. The DATA GATE (A) and SHIFT/LOAD are sent to the memory data output register as control signals. The ANALY STROBE is sent to the AM detection self-test control circuit, and the ROM CLK is sent to the fault count module to enable the UP COUNT.

13-65. The first test performed is the BIT analysis self-test. During this test the performance of the fault detection circuits is tested. The test circuits are enabled and all tuning units are intentionally programmed to cause fail conditions. A FAULT INDICATION INHIBIT is applied to the fault detection module to prevent fail indications during the test sequence. As each tuning unit is addressed, failure inputs from the am analyzer and amplitude test circuits on the AM and FM detection modules are gated through the addressable latch on the AM detection module. Lack of

a fault at the output of the addressable latch gates a fail to the self-test control circuit to enable the SELF-TEST FAULT. The SELF-TEST FAULT is sent to the fault count module. The fault count module processes the SELF-TEST FAULT so a fail condition is enabled only after three consecutive occurrences. On the first and second occurrence the test is re-initiated through the MEMORY ADDRESS CLR, SELF-TEST FAULT RESET, and UP/DOWN COUNT. On the third occurrence a SELF-TEST FAULT is sent to the fault detection module to enable fail indications. The FAULT INDICATIONS INHIBIT is inactive at this time. MEMORY BIT 5 resets the counter on the fault count module.

13-66. The second test performed is the manual mode PROM data and parity test. This is a test of data in the programmer ROM which controls the Oscillator in manual mode. The test is made up of a test for the existence of data and a test for correct data parity. The memory tells the command logic module to enable the manual mode PROM. The command logic module sends the PROM DATA ENBL, PROM DATA, DATA ENBL, and PARITY FAIL signals to the control module PROM data test and parity test circuits. The PROM DATA ENBL signal starts the test. A PRGMR ROM DATA FAULT is produced if the data ENBL input is active and PROM DATA is not available, and if a PARITY FAIL occurs when the DATA ENBL is active. The PRGMR ROM DATA FAULT is sent to the fault count module. The fault count module processes the PRGMR ROM DATA FAULT and sends a PROM DATA FAULT on the third occurrence to the fault detection module to enable fail indications. On the first and second occurrence of the PRGMR ROM DATA FAULT the test is re-started through the MEMORY ADDRESS CLR and UP/DOWN COUNT. MEMORY BIT 5 resets the counter after the third occurrence.

13-67. The third test performed is the tuning unit analysis test. During the test all tuning units are sequentially programmed to provide RF outputs with mod 1, 2, 4, and 5 modulation formats. BIT BINARY DATA from the memory is processed by the command logic outputs WORD LOGIC commands to program the tuning units. The memory sends MOD 1, 2, 4, and 5 TEST ENBL signals to the respective test circuits. Also, the TU ON and TU ADDRESS AA0, AA1, AA2 are sent to the AM Detection module as control signals. Failures detected by the AM Analyzer on the AM Detection module and the amplitude test circuits on the FM Detection module are gated to the addressable latch on the AM Detection module and also to the fault count module by way of the TU analysis fault detection circuit. The Fault Count module counts the occurrence of the TU ANALY FAULT. On the first and second occurrences the test is re-started by the UP/DOWN COUNT and MEMORY ADDRESS CLR control signals. On the third occurrence, the addressable latch on the AM Detection module is enabled and sends fault signals to the respective TU no. 1 through TU no. 8 fault logic circuits. Each tuning unit fault logic circuit validates the fault if circuit interlock exists. This prevents the BIT from failing tuning unit locations not installed. A valid tuning unit failure is gated to the fault detection module as a TU ANALY FAULT to enable fail indications. Also, a TU ANALY FAULT is produced if the tuning unit oscillator fails. The tuning unit oscillator fails (OSC FAULTS) are detected by the ALC circuit within the respective tuning unit and gated to the TU fault logic circuit as an ETO FAULT to enable the TU ANALY FAULT, if a TU ON signal is sensed.

13-68. The last test performed is the RF Amplifier test. This test is started when the memory sends the RF PWR TEST ENBL signal to the control module. The control module sends an RF AMPL BIT ENBL signal to the RF Amplifier set control module (see Figure 13-5). The RF AMPL BIT ENBL applied to the set control module overrides the WEIGHT ON WHEELS input to enable the RF Amplifier system circuits. BIT BINARY DATA from the oscillator memory is processed by the command logic module. WORD LOGIC commands produced by the data processors in the command logic module enable TU no. 1. The RF output from TU no. 1 is used to drive the RF Amplifier during BIT. Failures detected during BIT are gated to the set controls module to enable fail indications.

13-69. Intermittent BIT. Intermittent BIT can only be accomplished with the ICMS in the auto mode. Intermittent BIT is started by a specific digital message from the RWR and may be stopped by the RWR at any time by transmission of any other correct digital message. During intermittent BIT the same tests are performed as during initiated BIT except the RF power test and the BIT analysis self-test are not done.

13-70. The Oscillator Command Logic module, upon receiving the start intermittent BIT message from the RWR, produces the INTERMITTENT BIT START pulse, which is applied to the control module to enable

BIT GATE (A), BIT GATE (B), the programmable trigger generator, and also to gate the SYSTEM CLK to the counter. The INTERMITTENT BIT GATE signal is applied to memory BIT ROM 1 to inhibit the BIT analysis self-test and RF power test. The intermittent BIT program is then done as during initiated BIT and continues until the RWR sends a correct digital message to stop the program. Upon receiving a stop intermittent BIT message from the RWR, the command logic module produces an INTERMITTENT BIT STOP signal which is sent to the control module to reset the intermittent BIT gate, stopping the program.

13-71. BIT Fail Indications. The fault detection module in the oscillator fault locator receives fault signal inputs from various BIT circuits during the performance of continuous, initiated, and intermittent BIT and produces fault signals to latch or light the applicable fault indicators. These fault inputs are classified as either oscillator faults or external faults. Oscillator faults are those resulting from some failure in the oscillator (VOLTAGE FAULT, SELF-TEST FAULT, PROM DATA FAULT, TU ANALY FAULT or MASTER CLOCK FAULT). External faults result from a failure of the RWR or the RF Amplifier.

13-72. Initially upon power turn-on and during system warmup, the ICS light on the BCP is on. The ICS light remains on until a CYCLE-IN GATE is produced and sent to the BCP no-go driver on the oscillator fault detection module. The BCP no-go driver holds relay K4 energized when the CYCLE-IN GATE is available and no faults exist. This action deenergizes relay K1 in the Avionics Miscellaneous Modular Relay Panel No. 3 causing the ICS light to go out.

13-73. During BIT, the oscillator faults are gated to the BIT latch driver, ASP 59 latch driver, BCP no-go driver, and the set no-go driver. The BIT latch driver enables the oscillator BIT fail indicator (black and white), the ASP 59 fault indicator driver enables relay K5 causing fail indicator 59 on the Avionics Status Panel to set (orange), the BCP no-go driver deenergizes relay K4 causing the ICS light to light on the BCP, and the set no-go driver enables relay K3 to light the respective SET-2 FAIL or SET-3 FAIL lights on the TEWS control panel.

13-74. External faults applied to the oscillator fault detection module enable the set no-go driver, and ASP fault indicator 59 driver. The RWR DATA FAIL or PARITY RATE FAIL enable the BCP no-go driver and set no-go driver to light the ICS light on the BCP and the respective SET-2 FAIL or SET-3 FAIL light on the TEWS control panel. RF Amplifier faults are sensed by the BIT circuits within the RF Amplifier and are applied to the RF Amplifier set control module to enable the AMPL BIT or ANT BIT indicator on the RF Amplifier. Also, an RF AMP FAULT is sent to the oscillator to enable the ASP fail indicator 59 driver and set no-go driver.

13-75. Failures sensed within the RF Amplifier are the ANTENNA FAULT, RF LEVEL FAULT, circuit INTERLOCK FAULT, THERMAL FAULT, MODULATOR FAULT, FINAL HVPS FAULT,and DRIVER HVPS FAULT. All RF Amplifier faults are gated to the fault counter/timer on the set control module. The fault counter/timer counts the occurrence and time of a specific fault input. Three faults within a specified time frame enable relay K5 on the set control module causing an RF AMPL FAULT signal to the oscillator and also disable the HVPS, ALC, and modulator by way of the turn on/off sequence generator. All fault inputs set the AMPL BIT indicator except the antenna fault. The antenna fault enables the ANT BIT indicator when the fault counter/timer has been satisfied.

13-76. **System Interface.** See Figure 13-8. The RWR sends data link and look-thru signals to the ICMS. The ICMS sends program request, ICMS status and a composite RF sample to the RWR system during auto mode of operation.

13-77. After the ICMS system initially times out or if power has been interrupted longer than 500 milliseconds, the ICMS sends a program request signal to the RWR system. Upon receipt of a program request, the RWR system sends a data link signal which identifies the frequency and modulation requirements required to jam detected threats. The ICMS processes the data link signal, sets up the required tuners, sends an ICMS status signal and a sample of the RF back to the RWR system for comparison.

13-78. When the RWR system must scan the frequencies which the ICMS is jamming, a look-thru. signal is sent to the ICMS to blank the transmitter until the RWR scans past that specific frequency. If the threat no longer exists at that frequency, the RWR system then commands the ICMS to shut down the tuner which was jamming that frequency.

13-79. If the RWR system, in comparing the sample

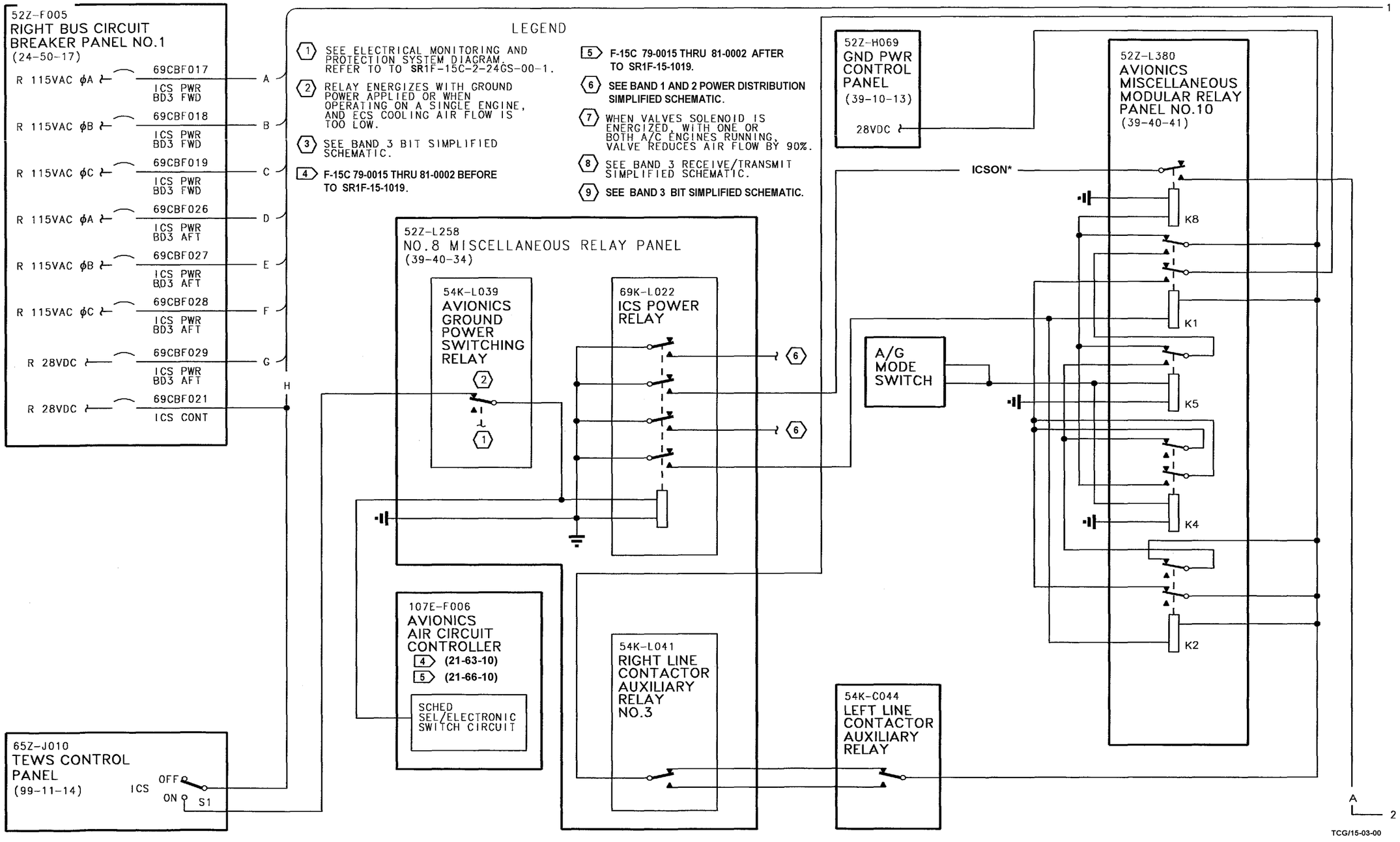


Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 1 of 7)

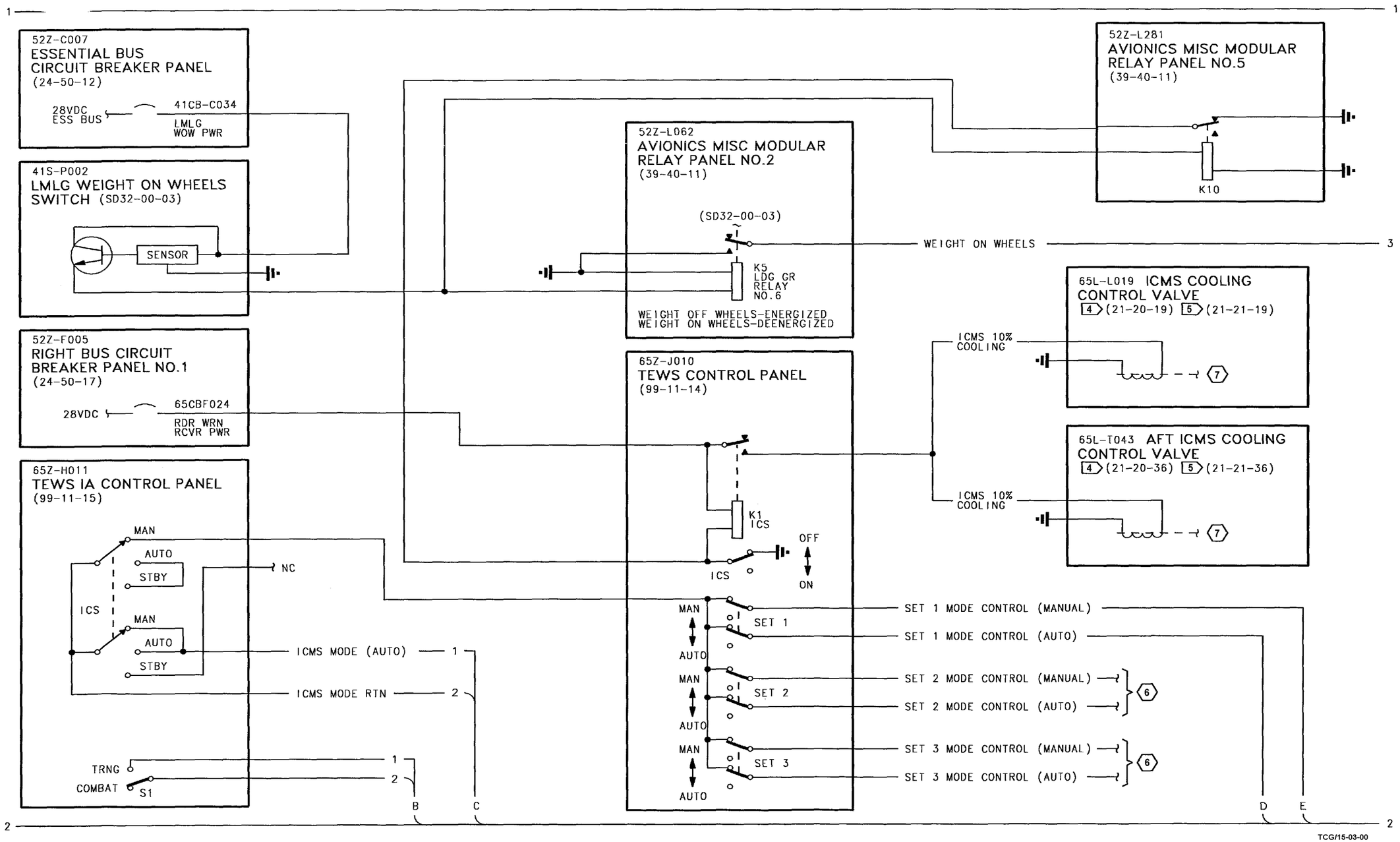


Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 2)

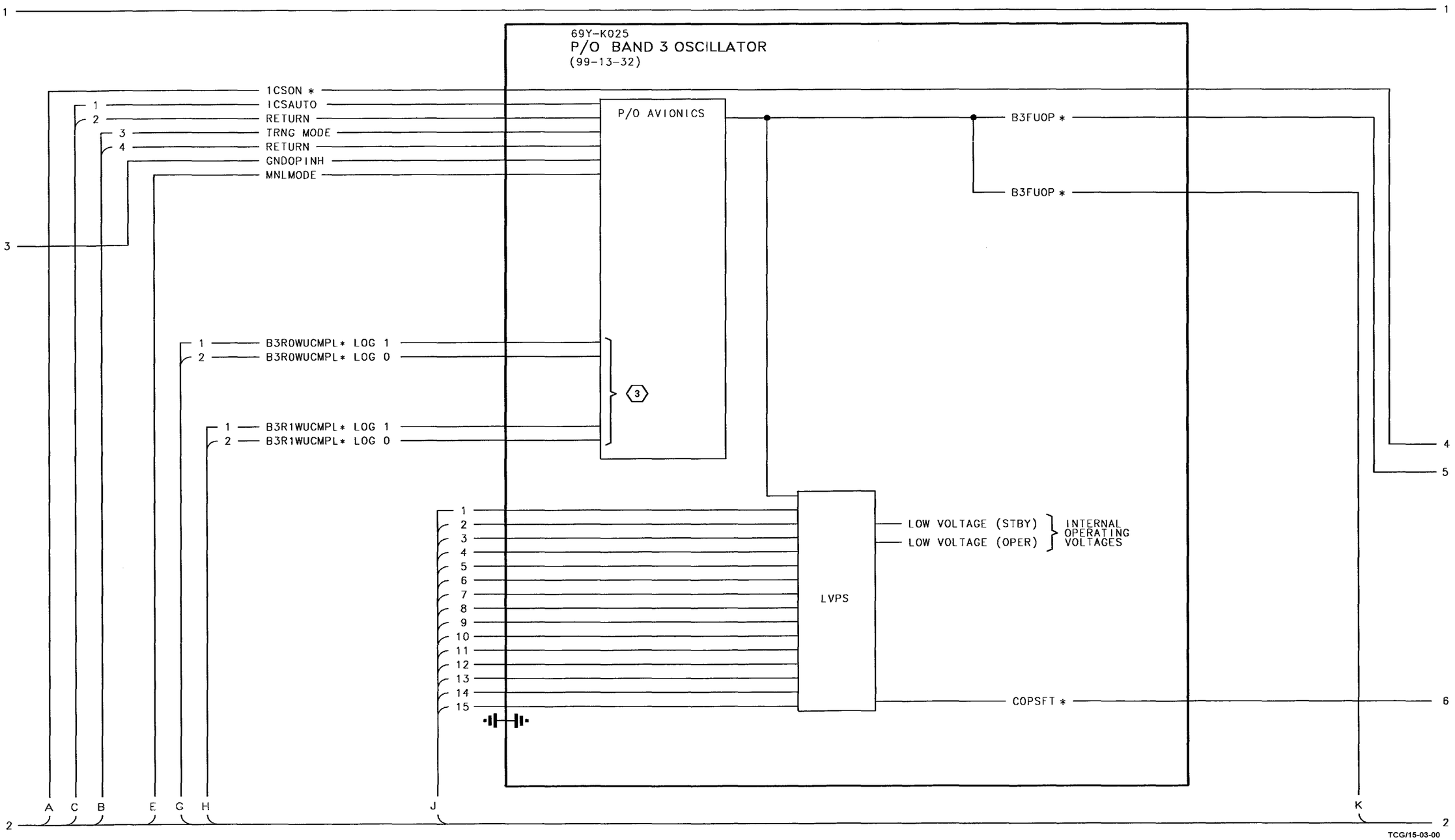


Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 3)

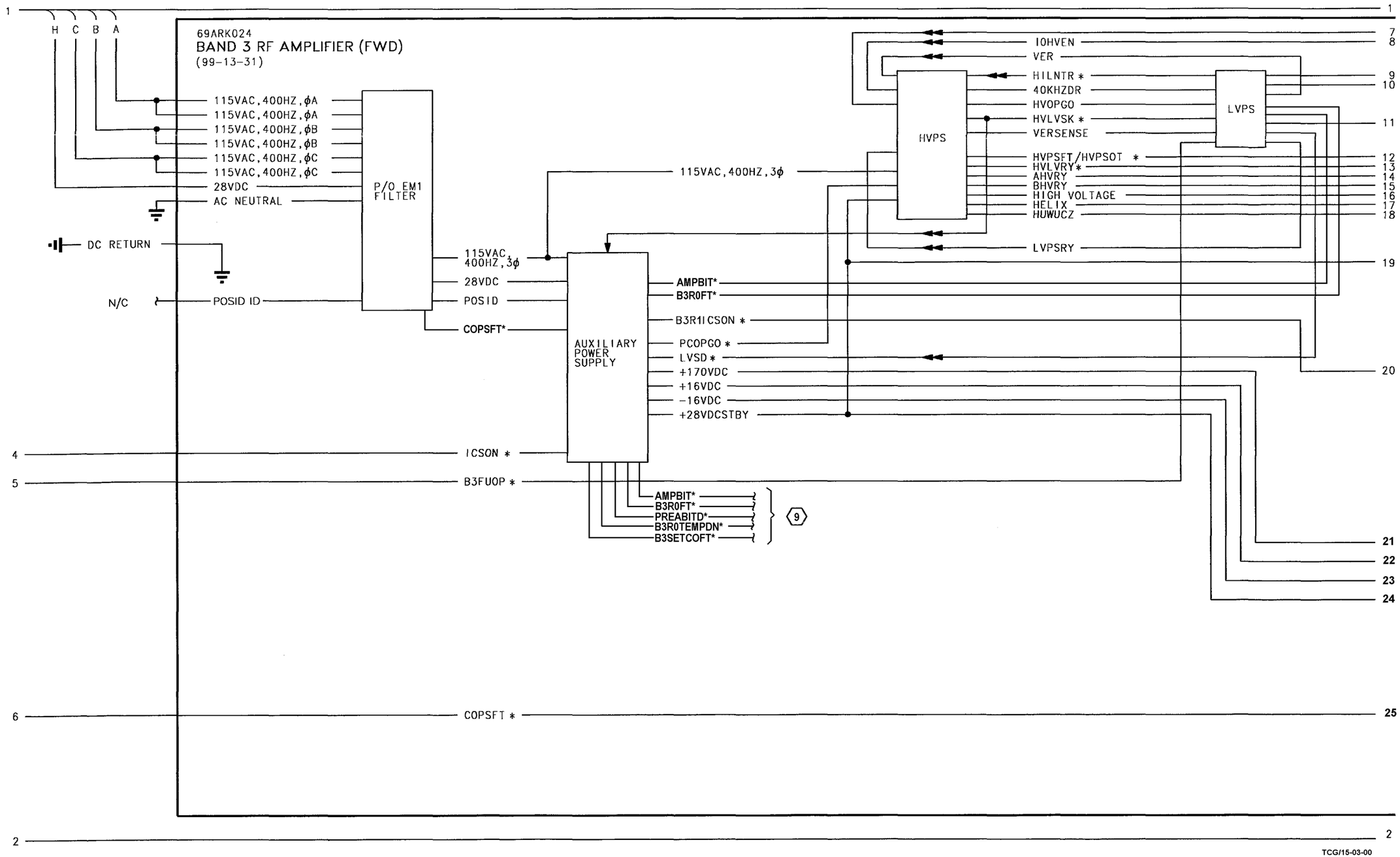


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Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 4)

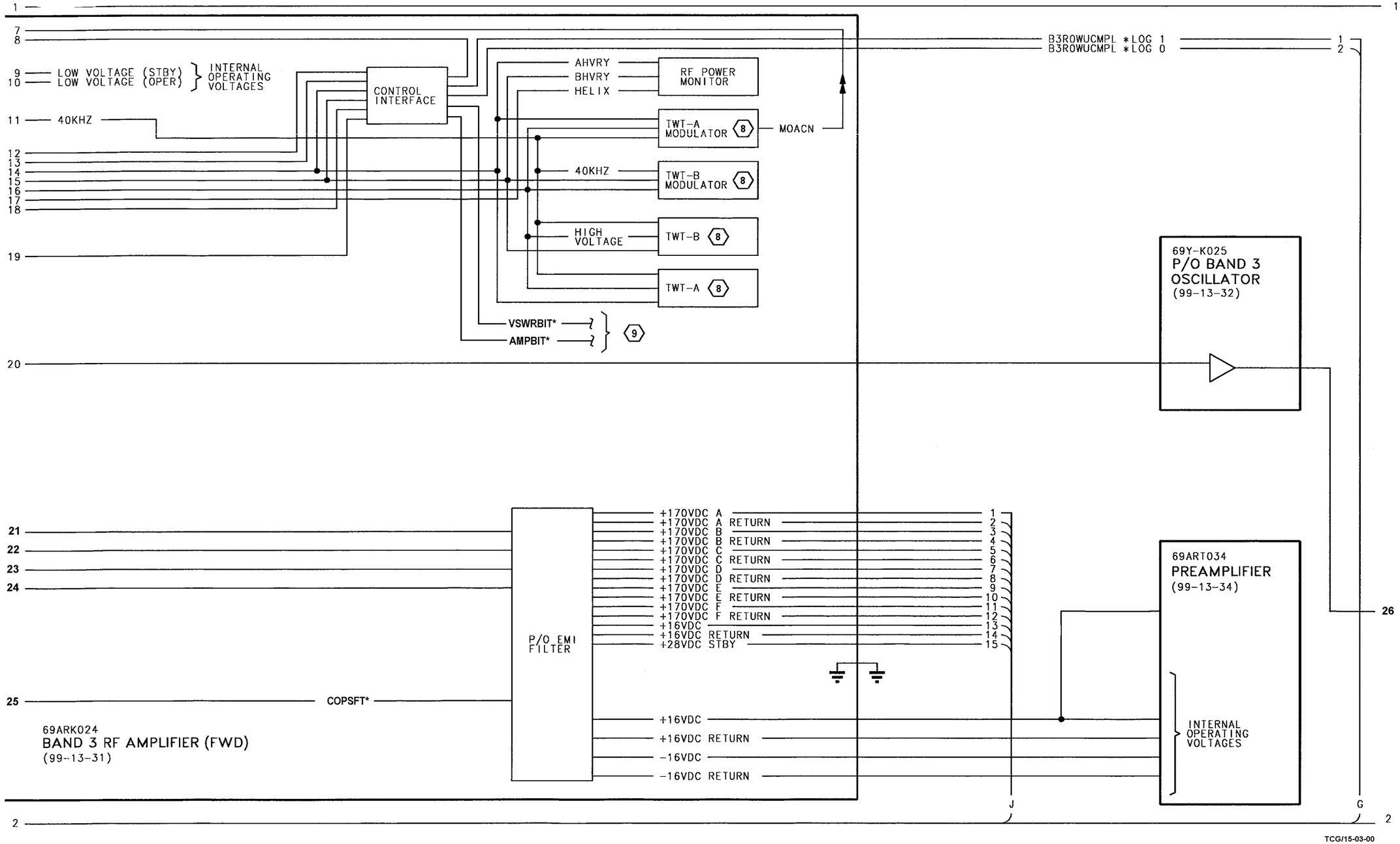

Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 5)

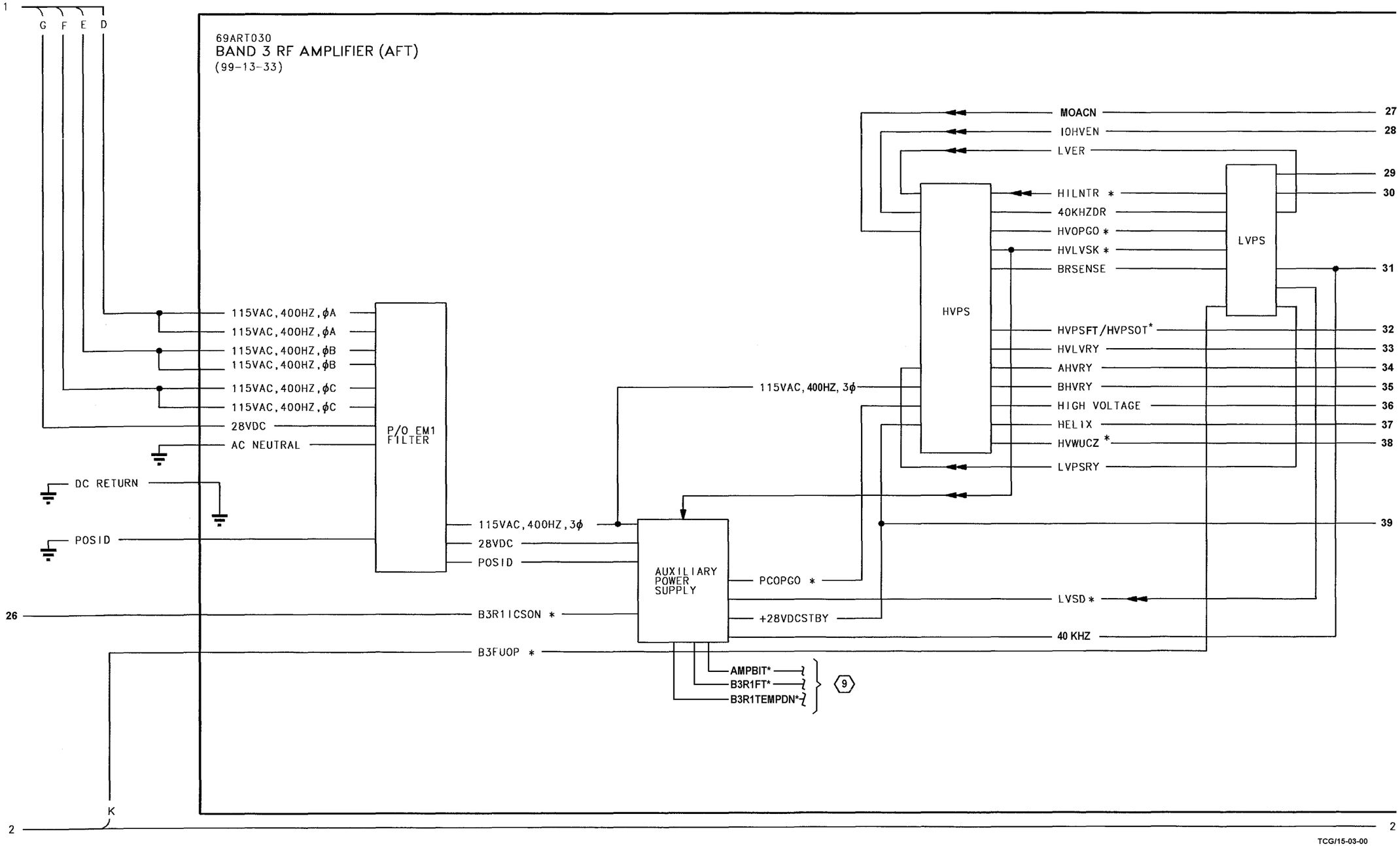

Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 6)

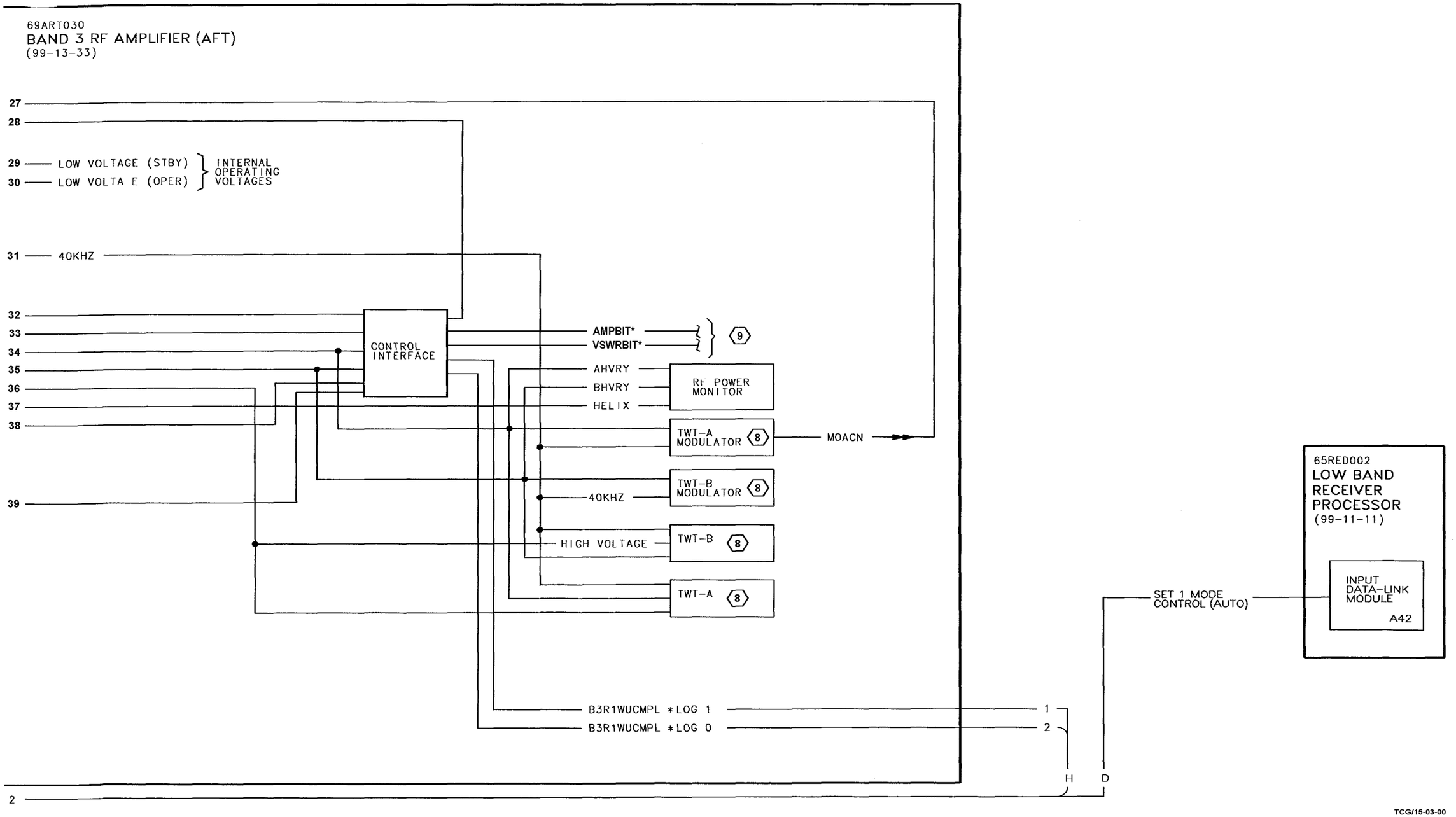

Figure 13-9. ICMS Band 3 Power and Control Simplified Schematic (Sheet 7)

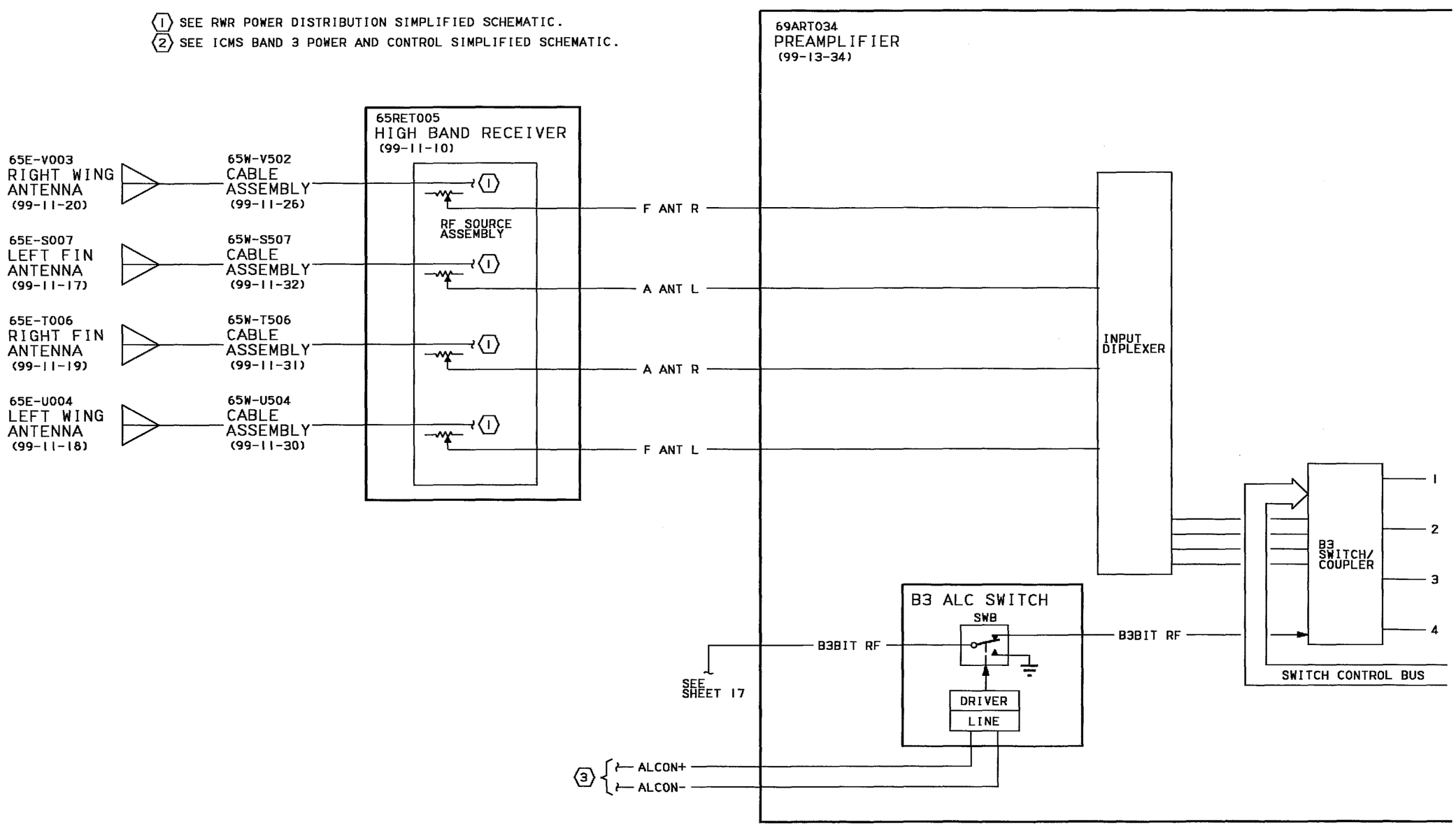

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 1 of 17)

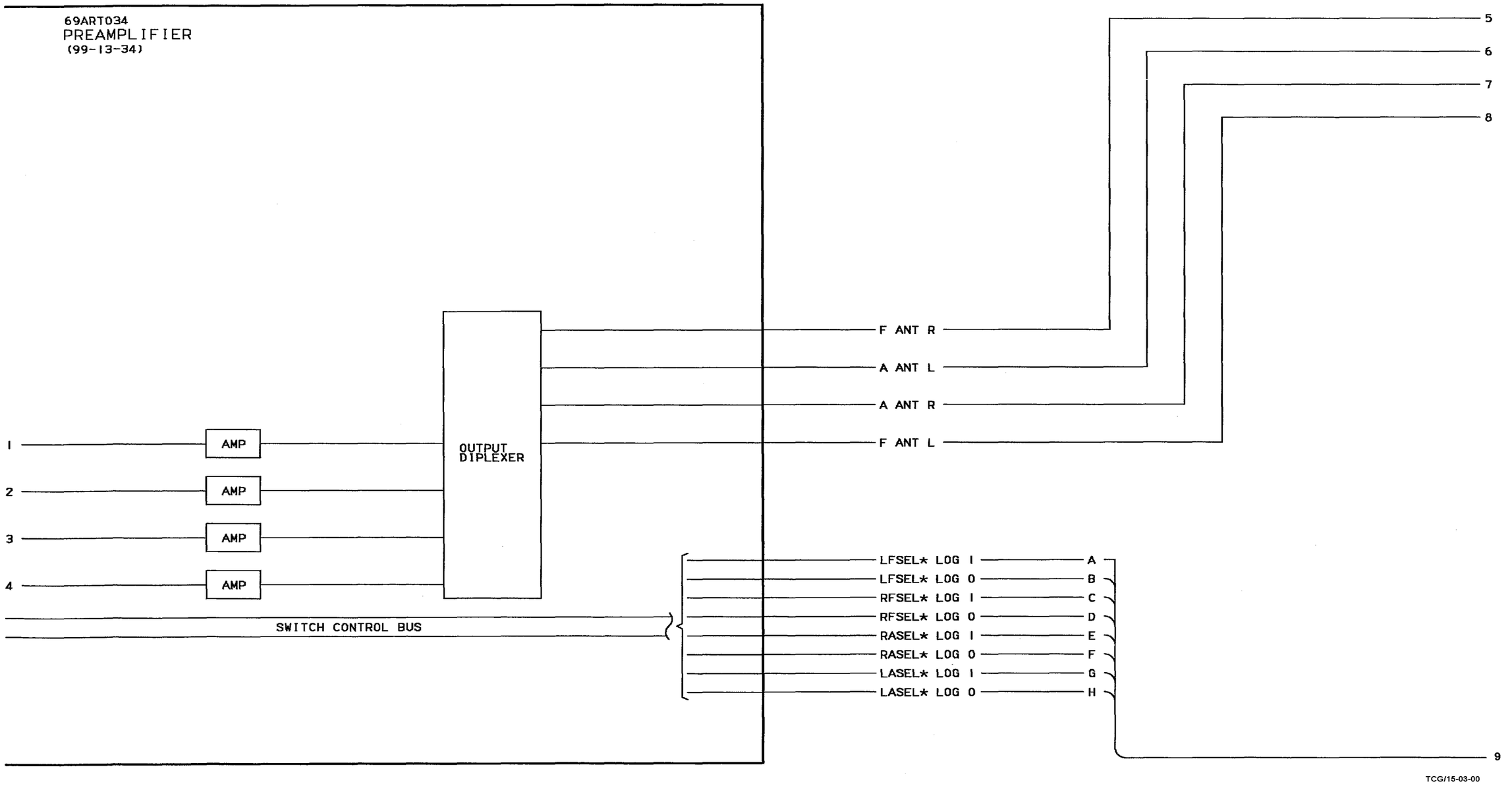

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 2)

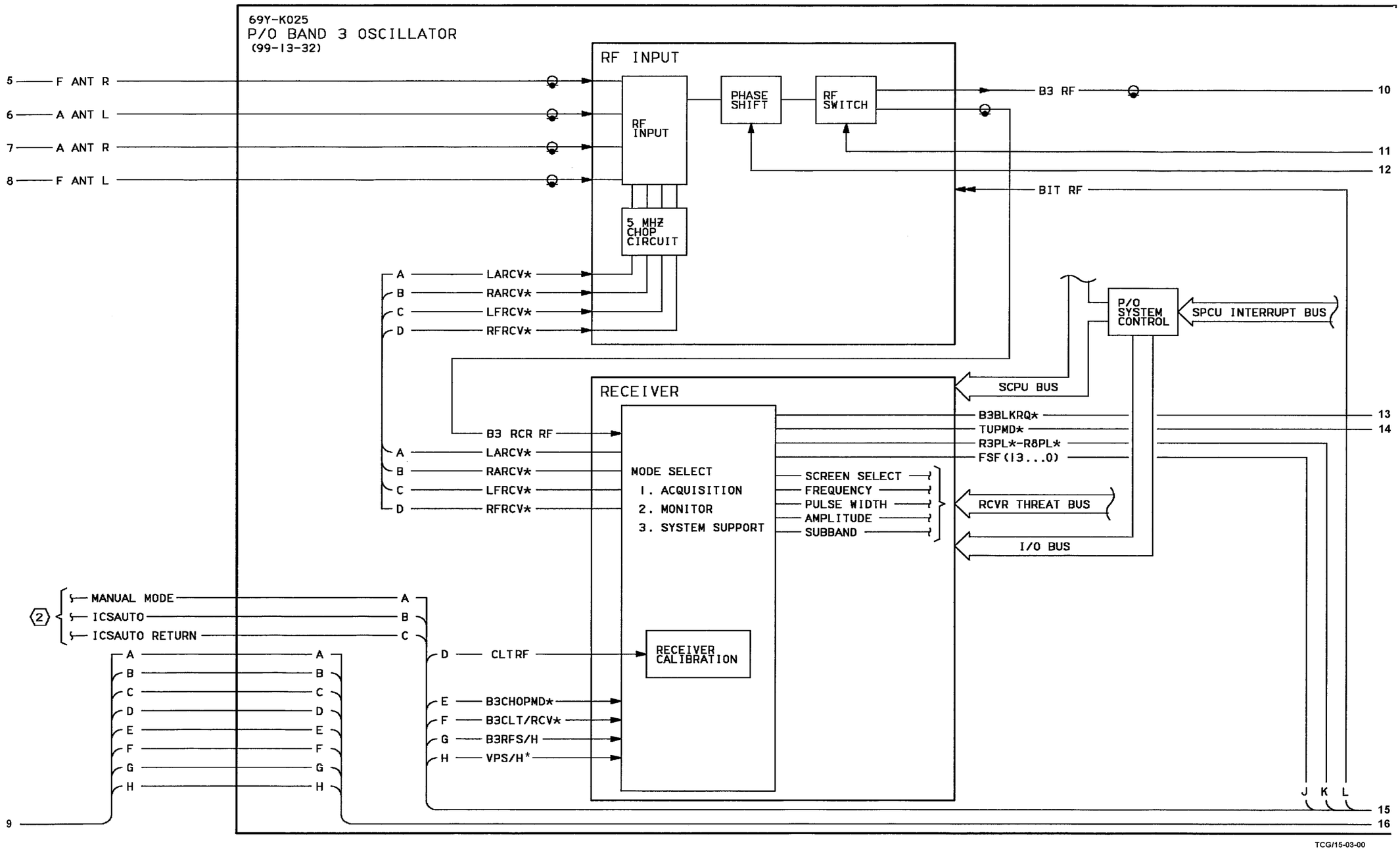

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 3)

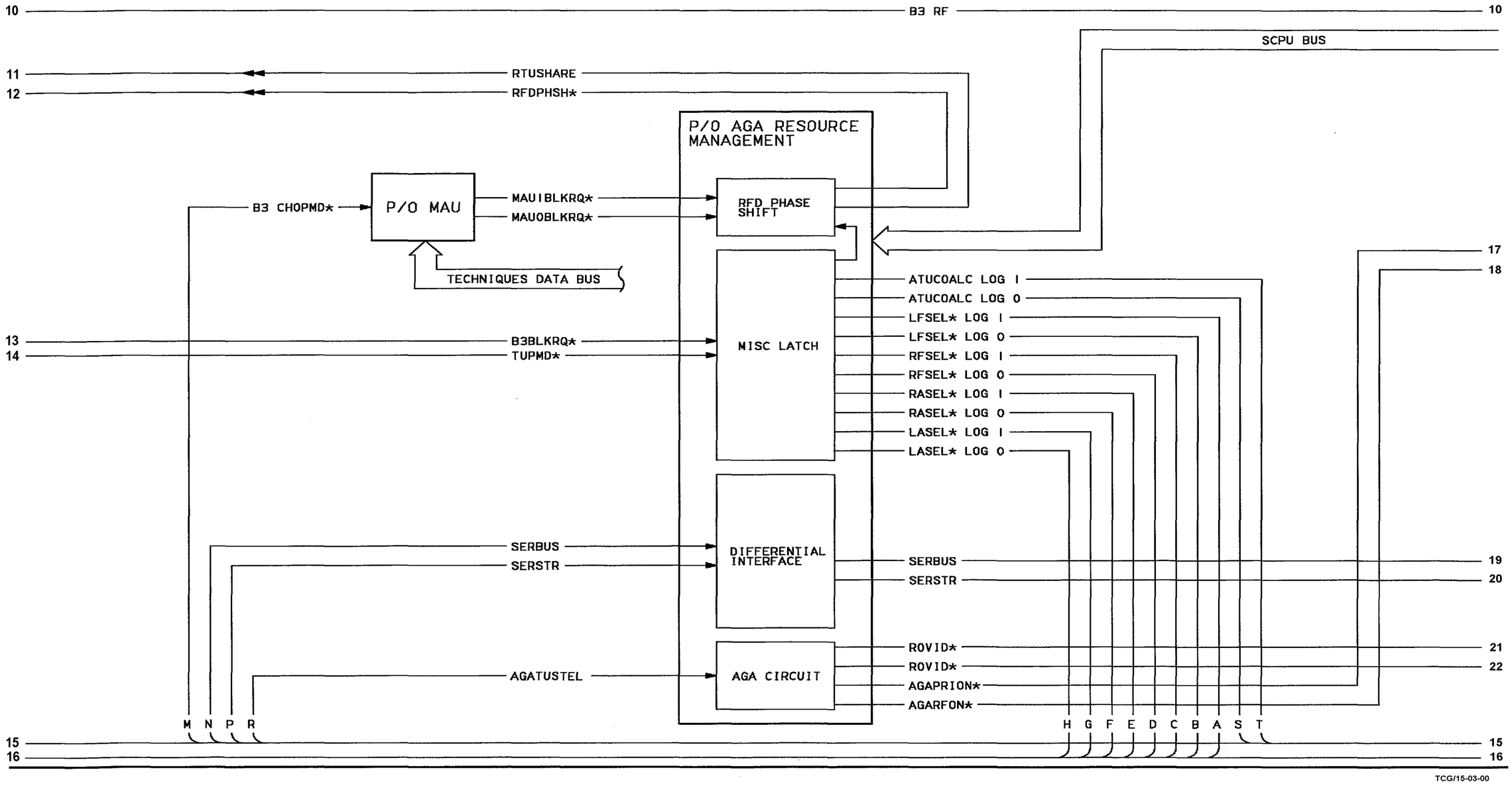

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 4)

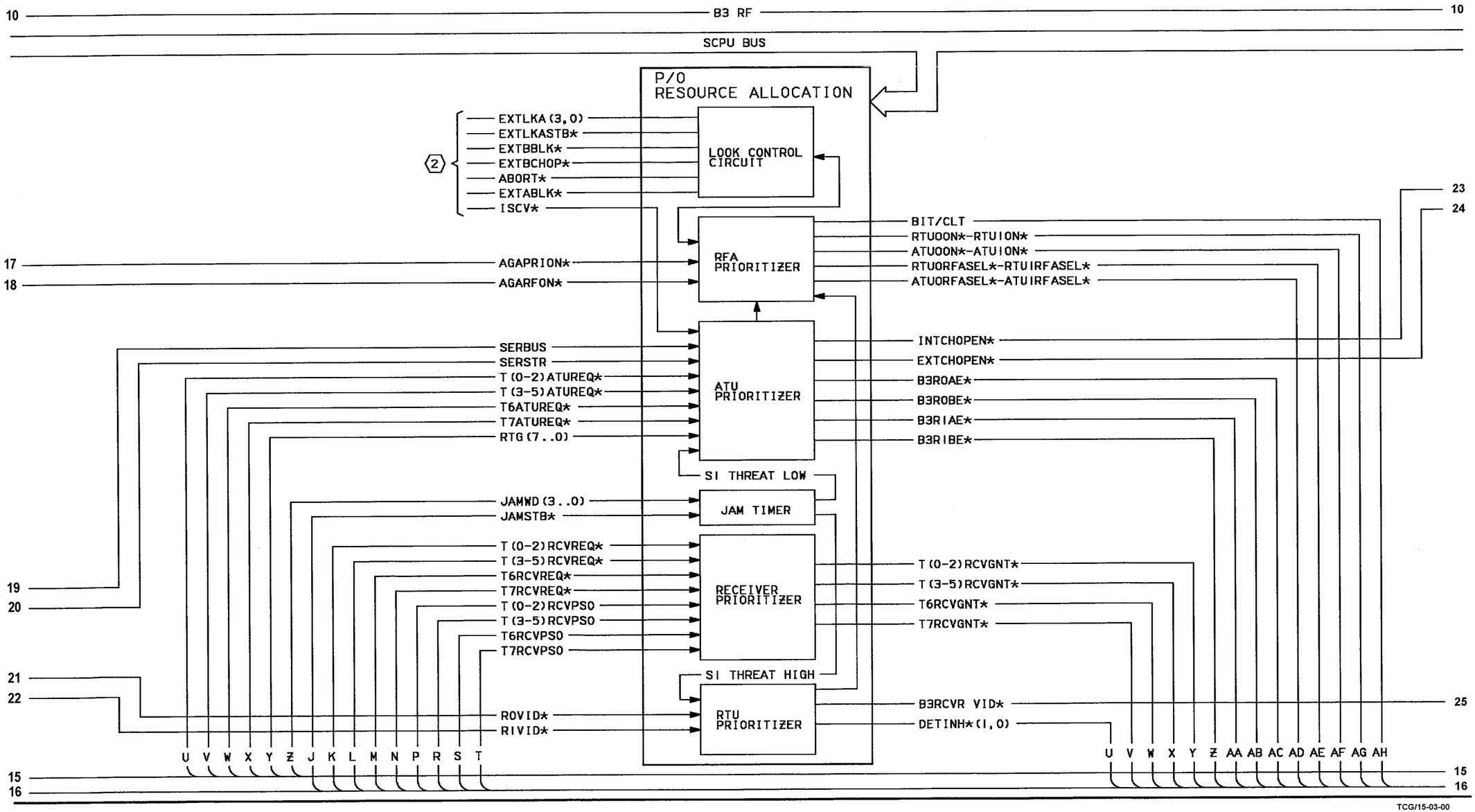

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 5)

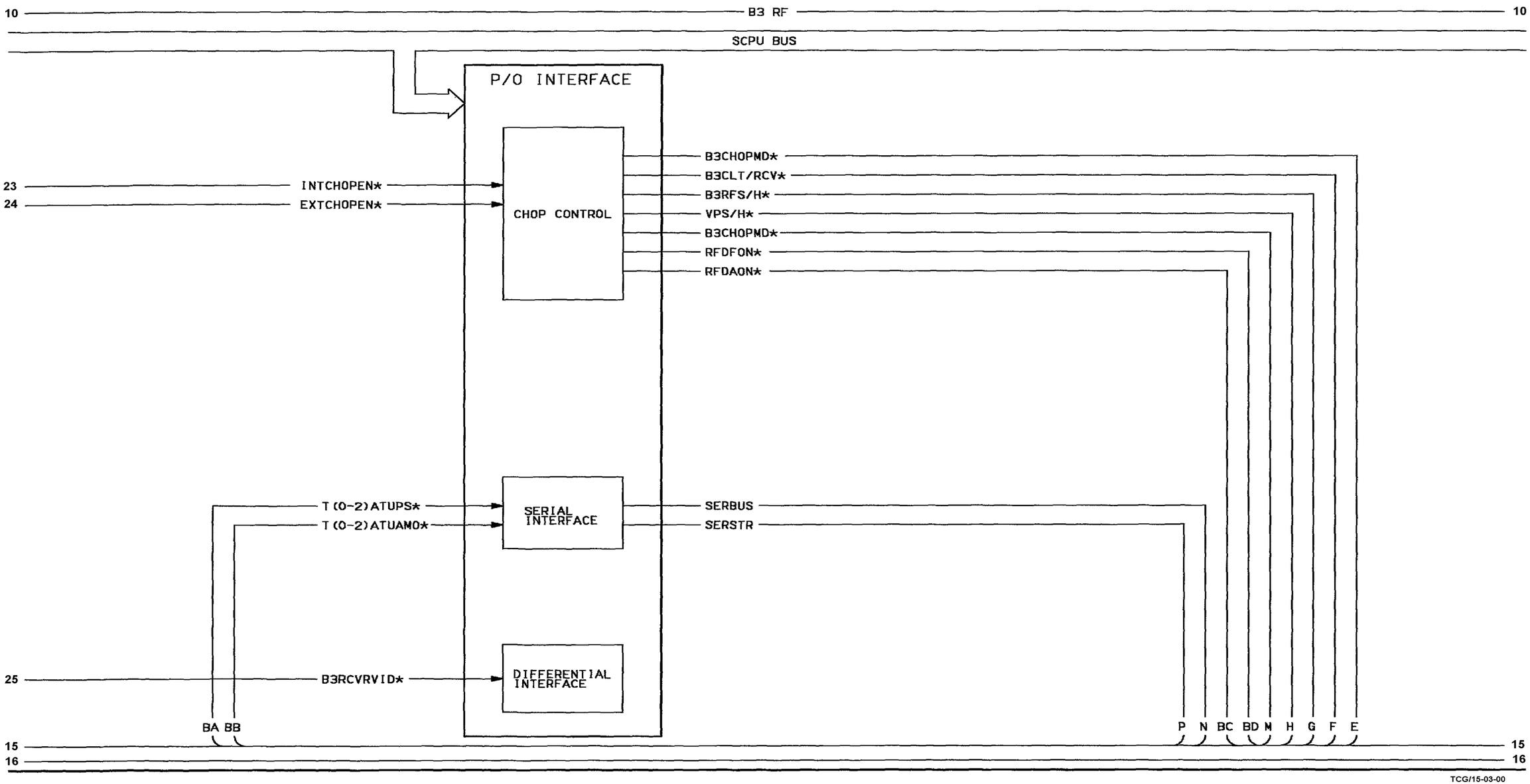

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 6)

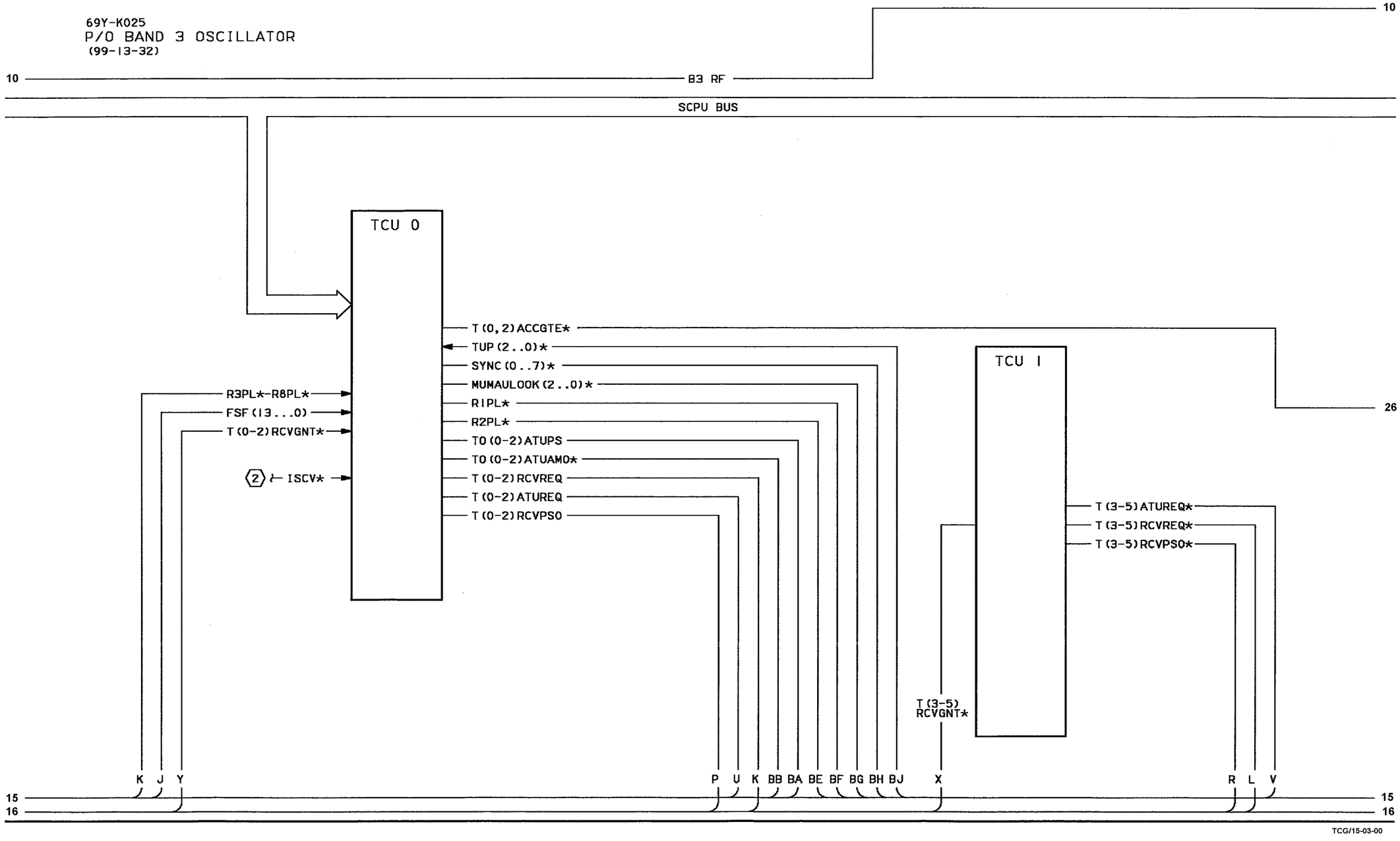

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 7)

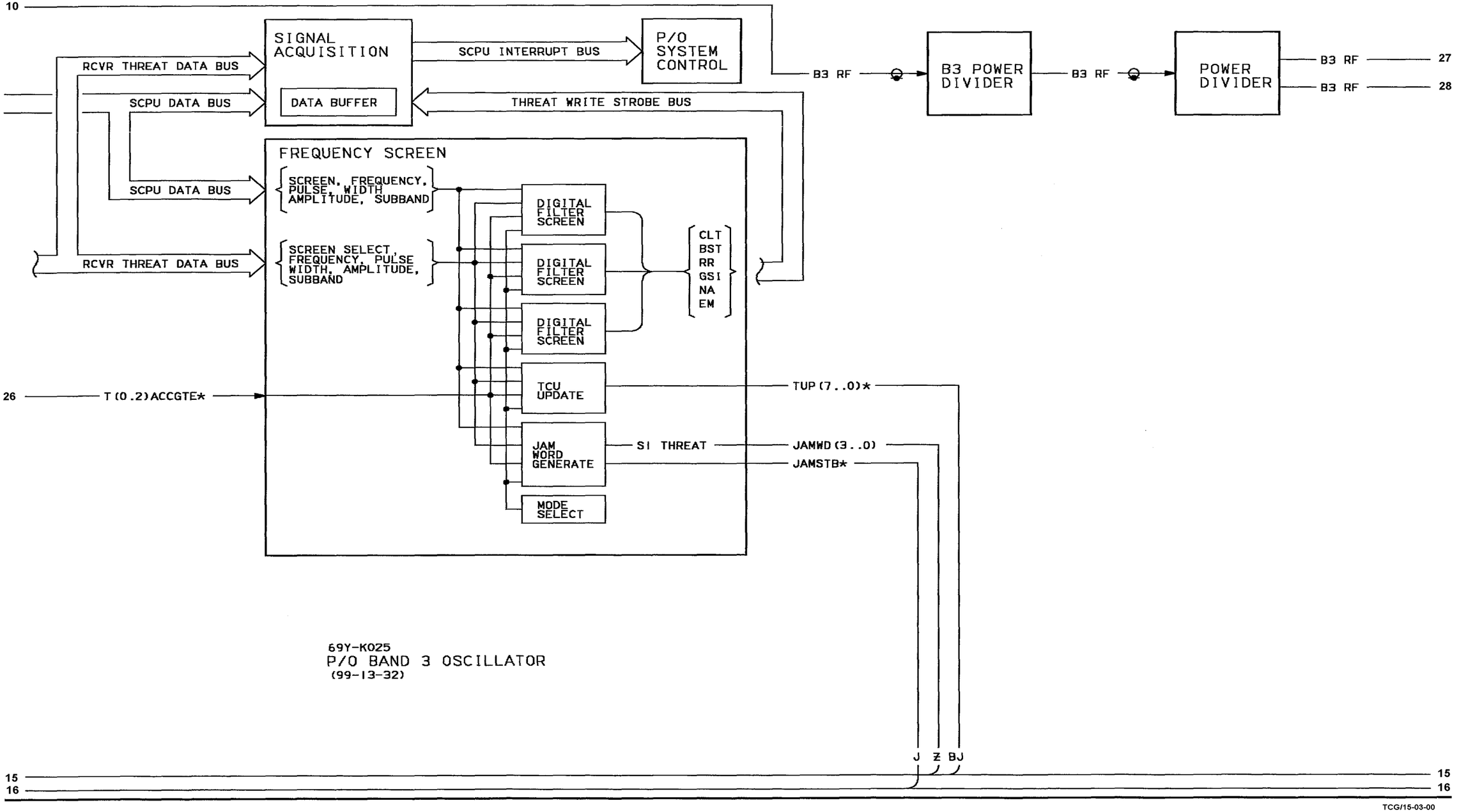

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 8)

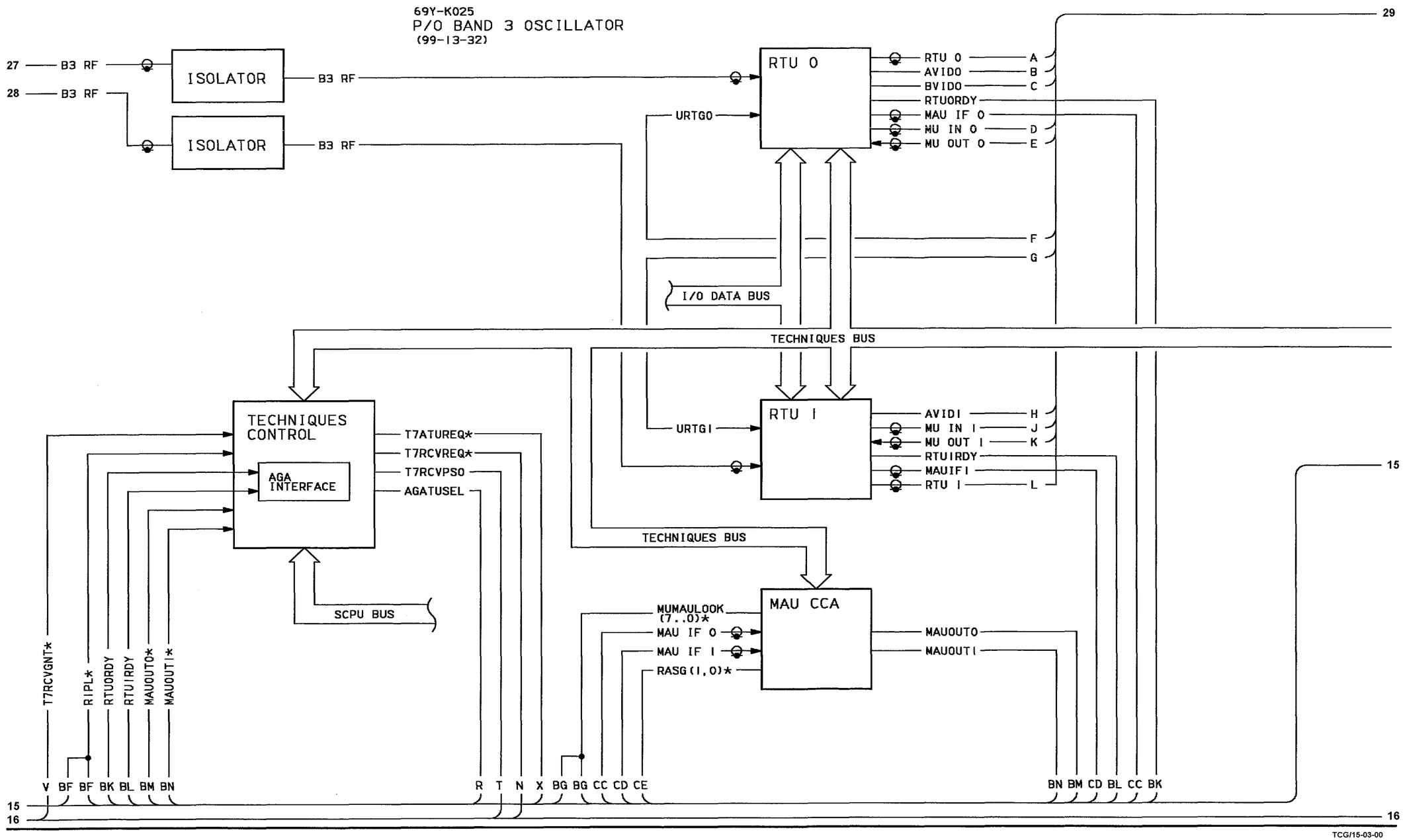

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 9)

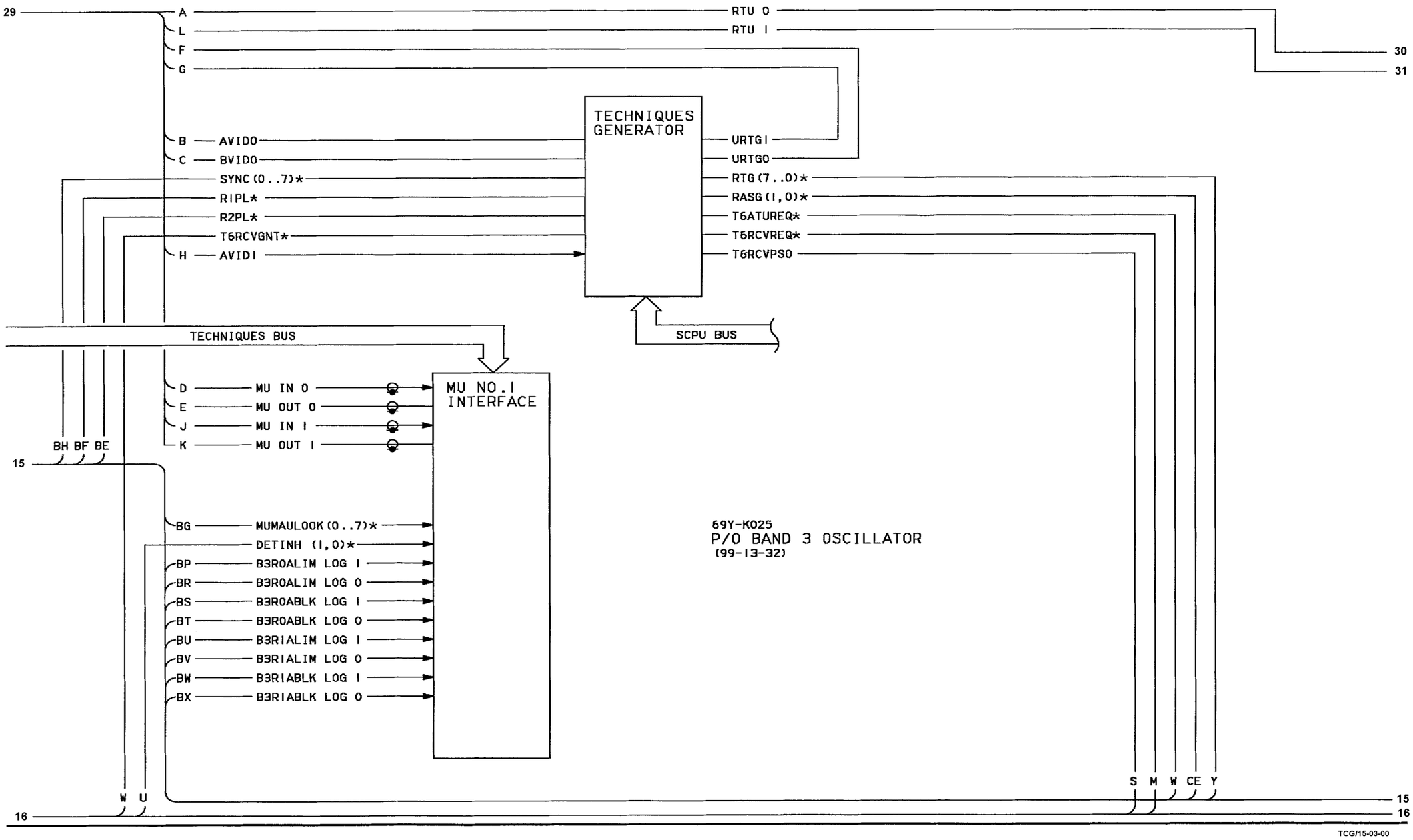

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 10)

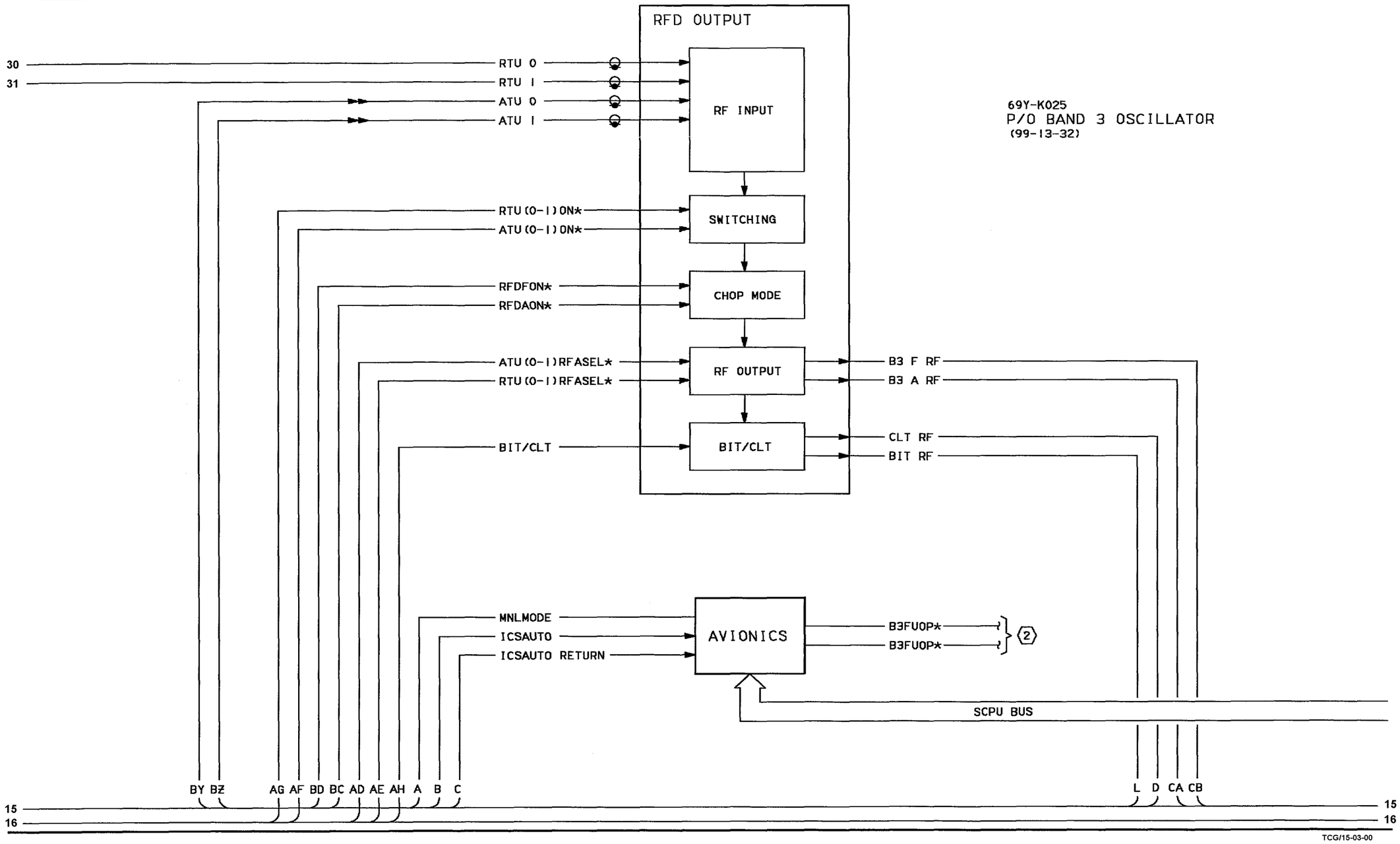

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 11)

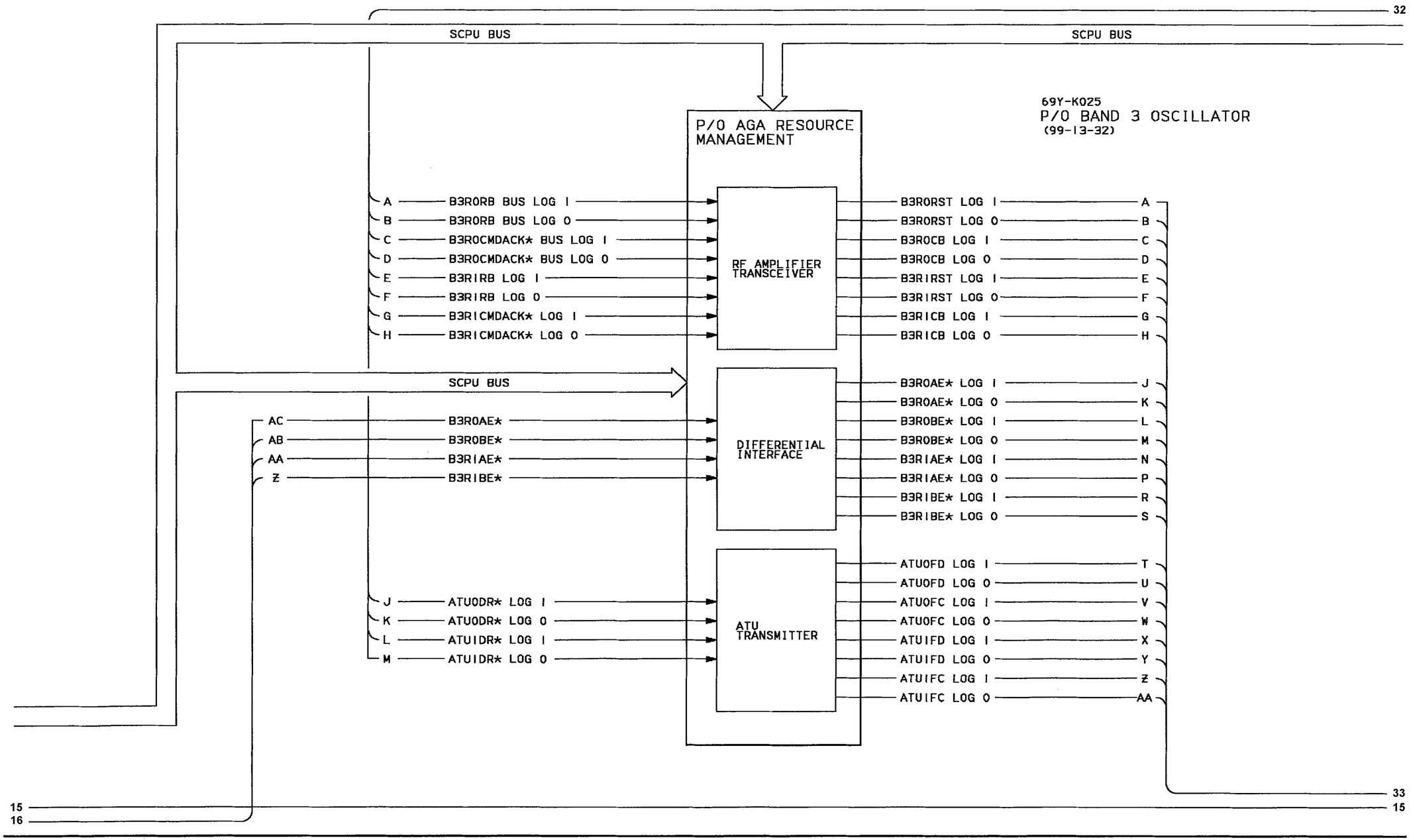

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 12)

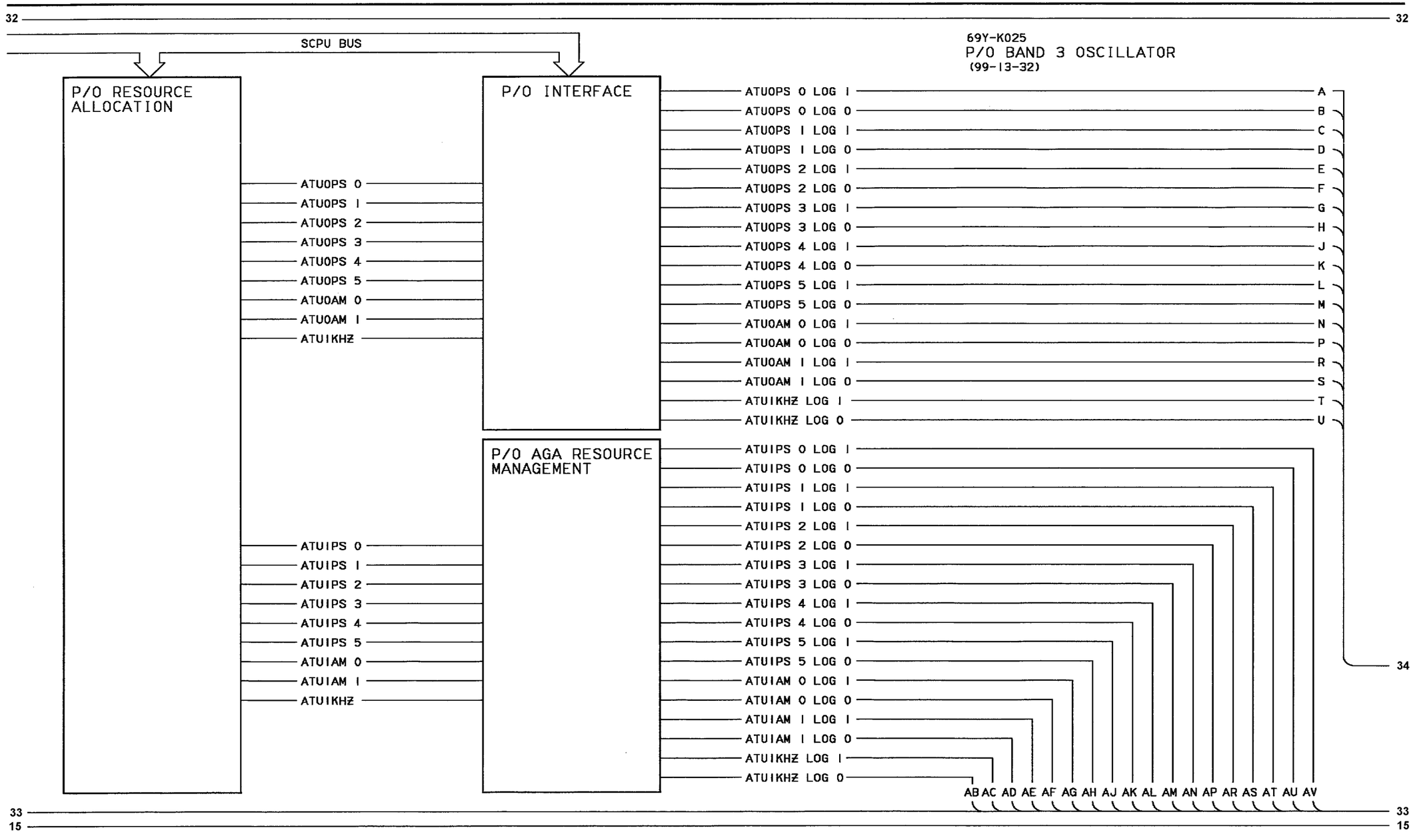

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 13)

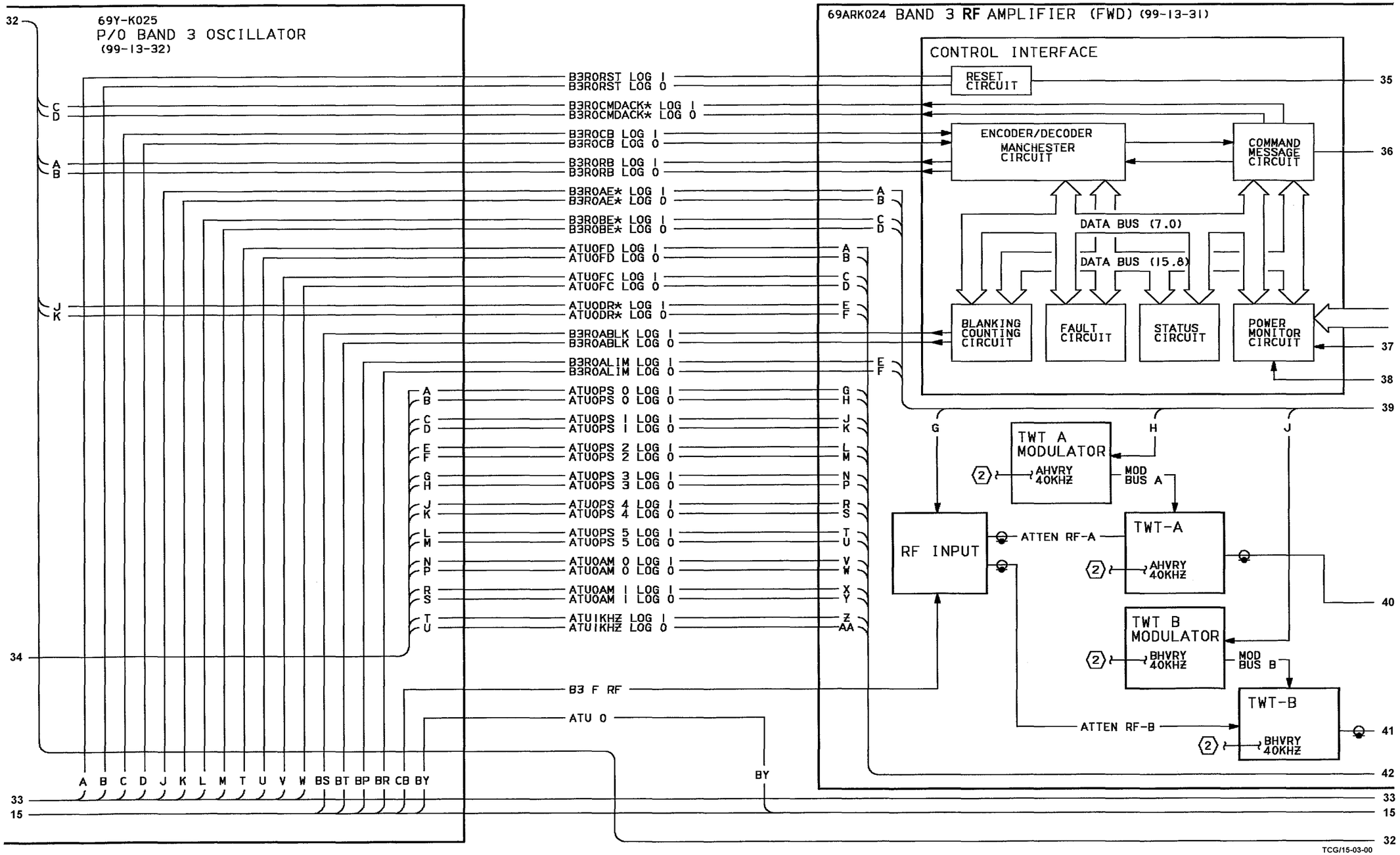

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 14)

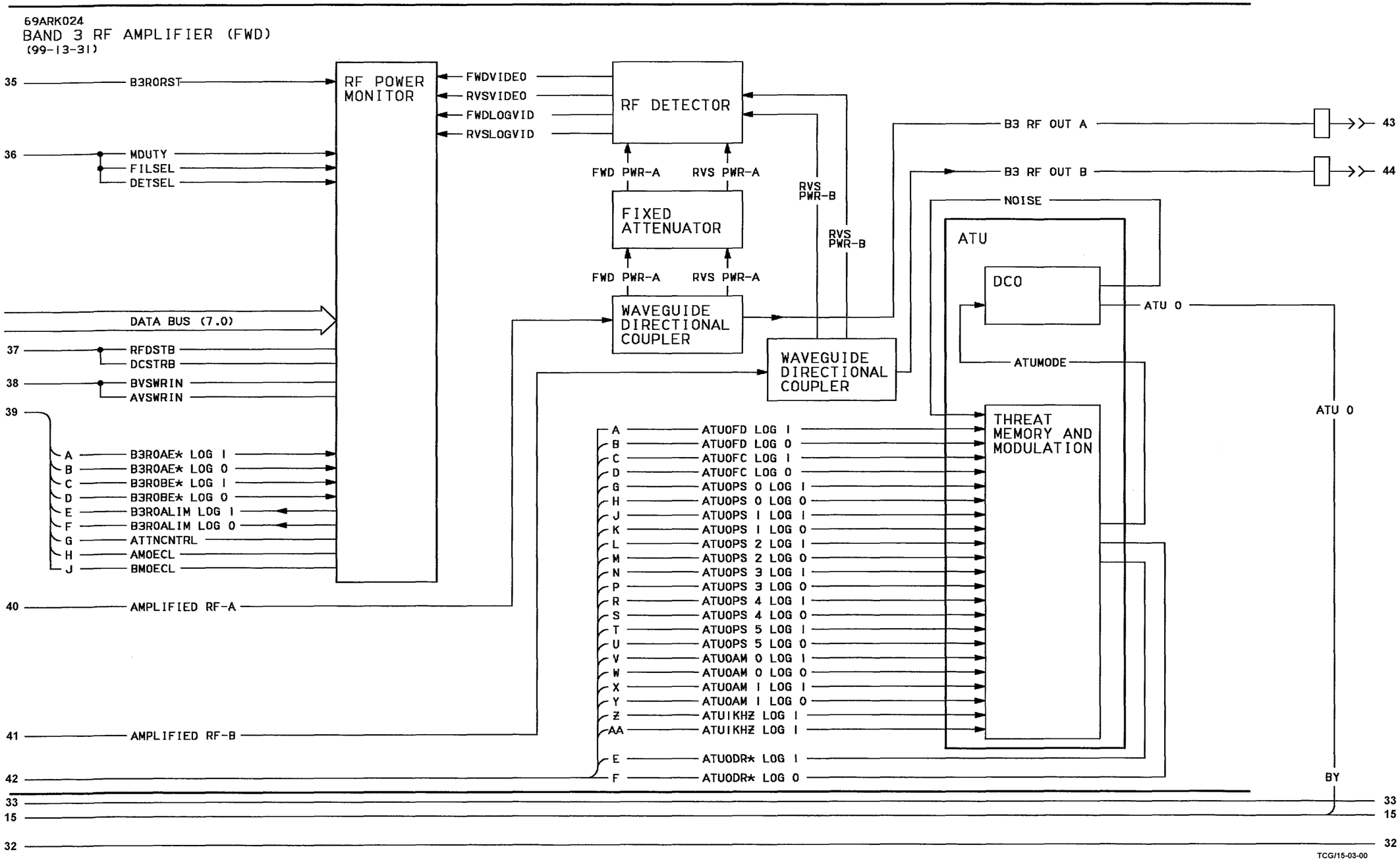

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 15)

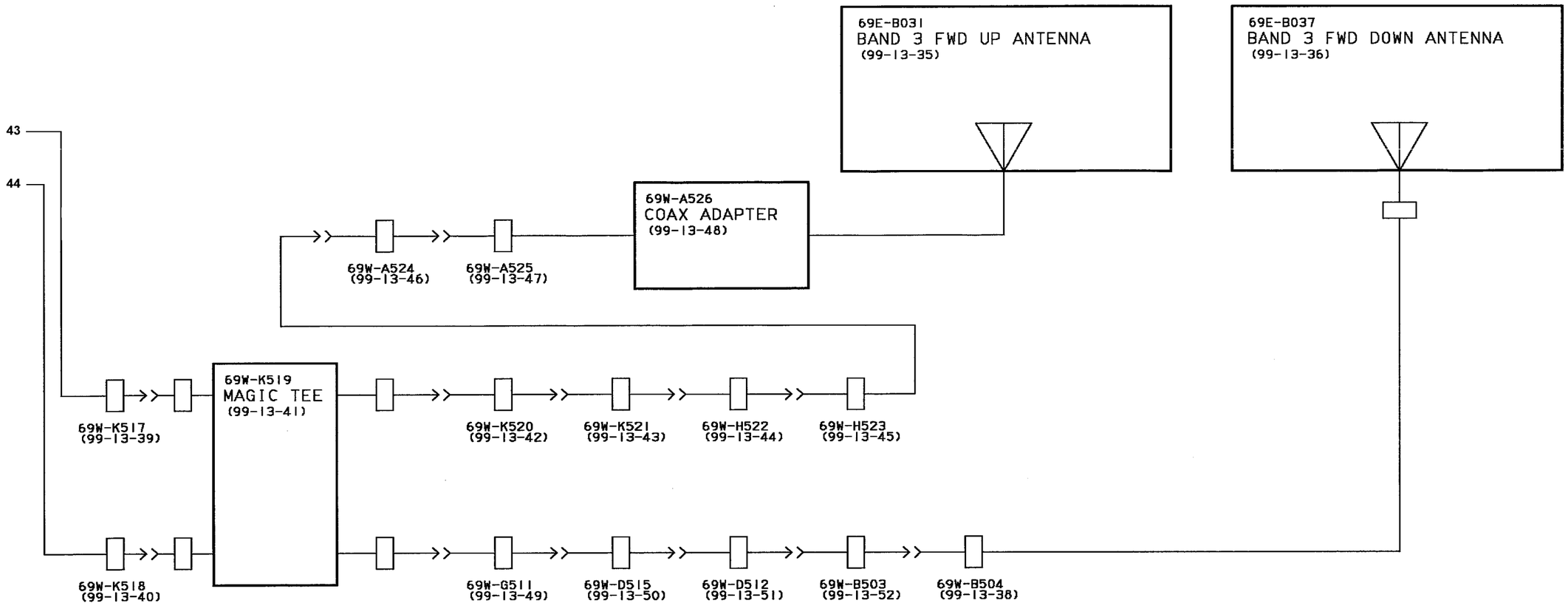

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 16)

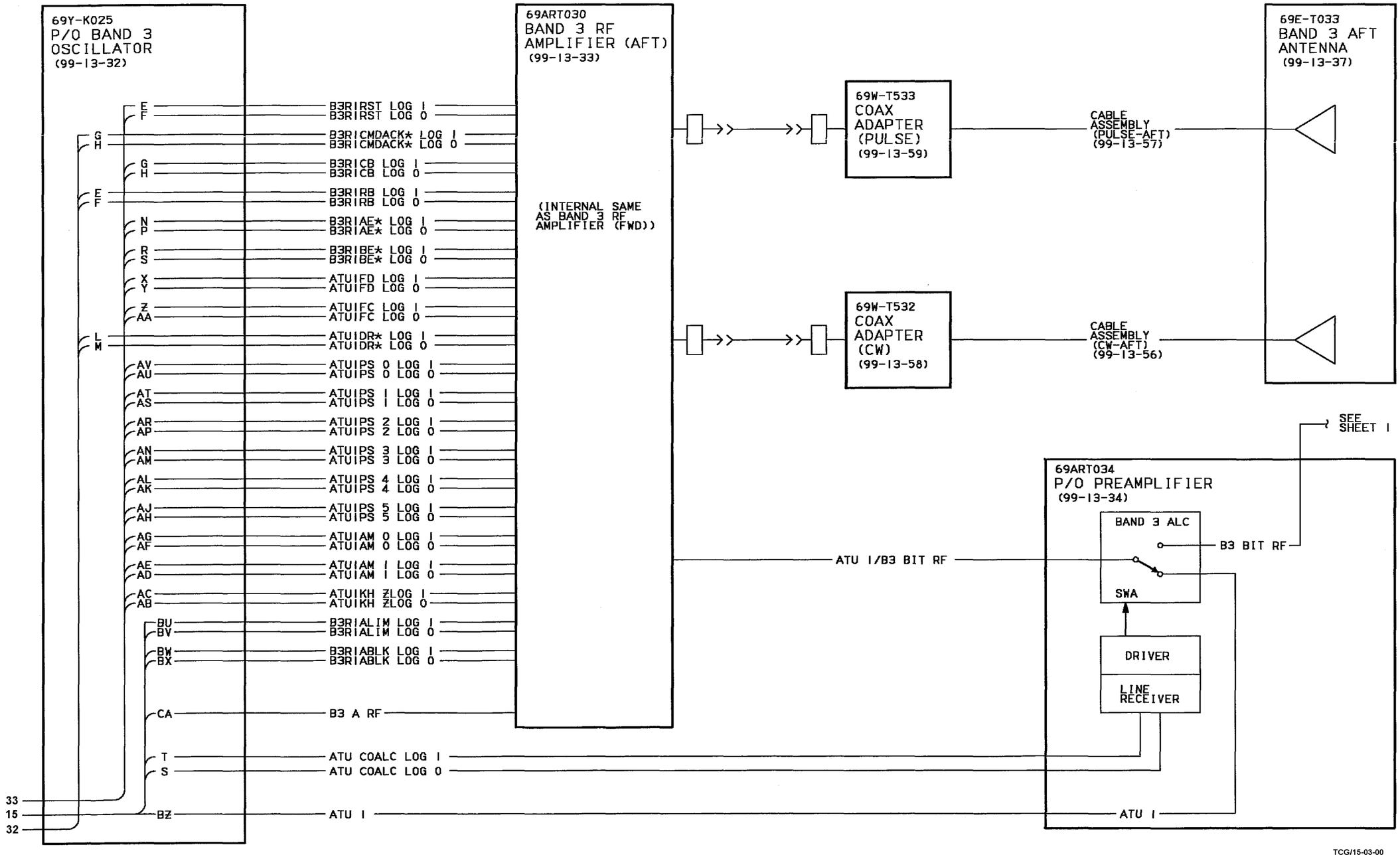

Figure 13-10. ICMS Band 3 Receive/Transmit Simplified Schematic (Sheet 17)

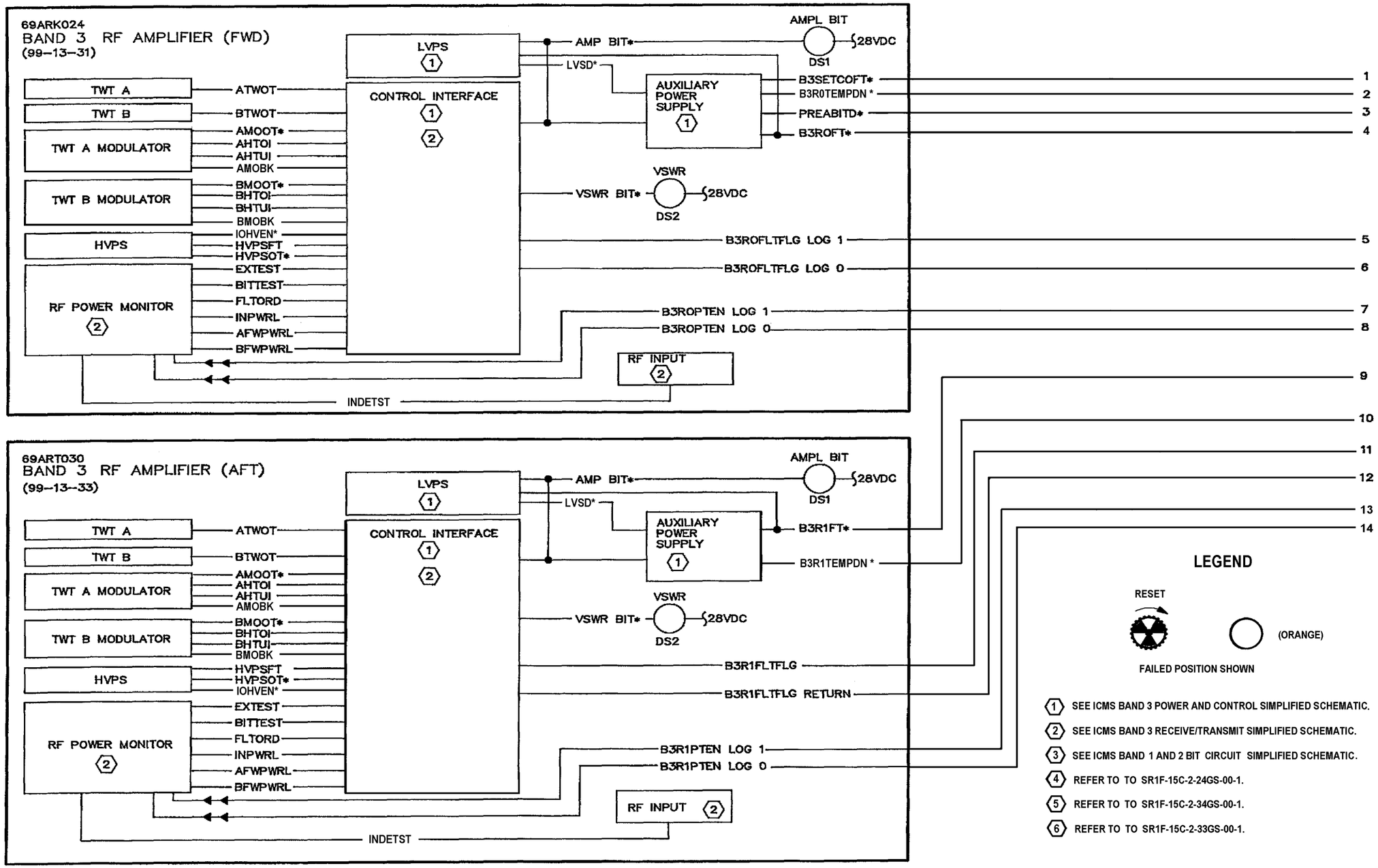

Figure 13-11. ICMS Band 3 BIT Circuit Simplified Schematic (Sheet 1 of 4)

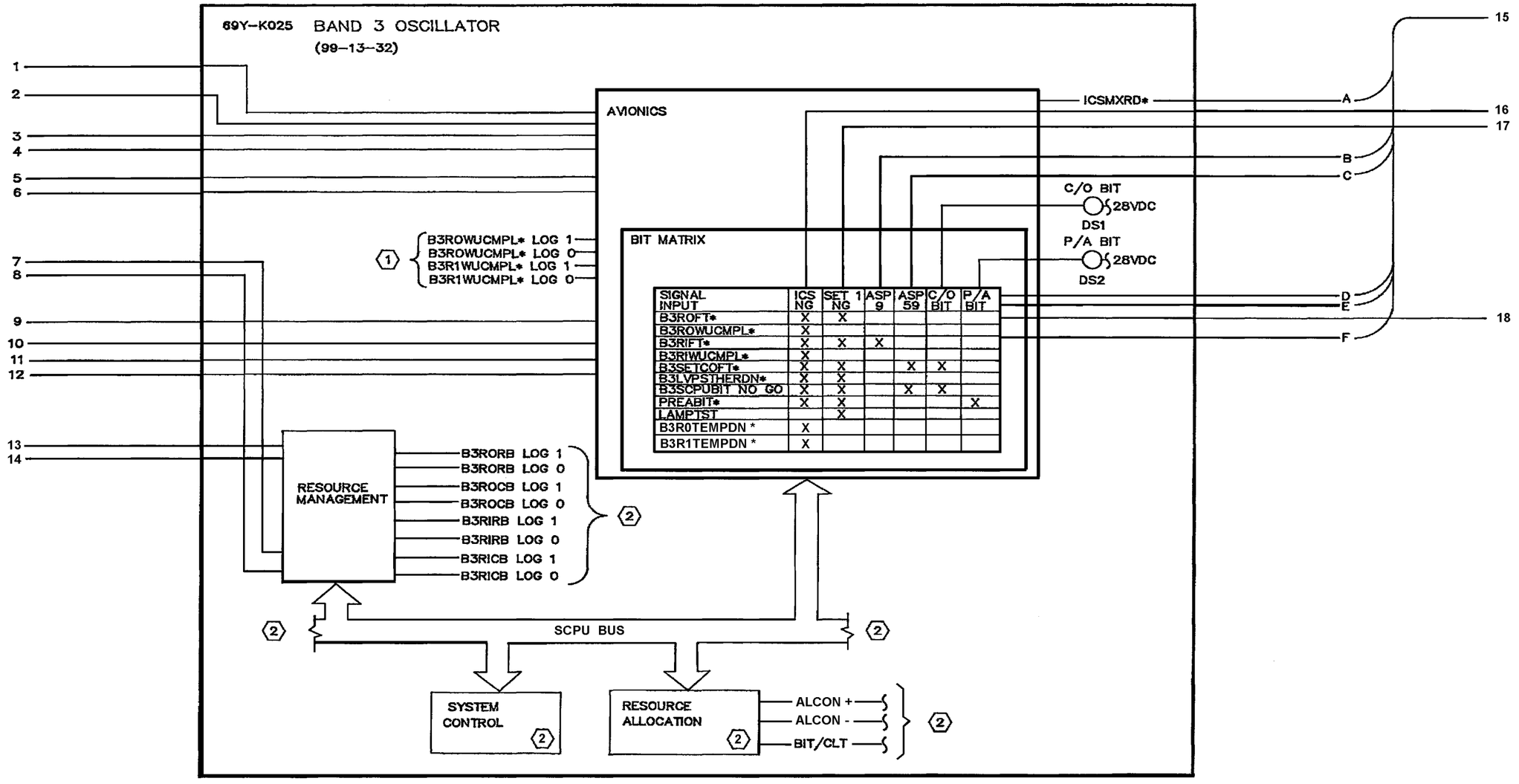

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Figure 13-11. ICMS Band 3 BIT Circuit Simplified Schematic (Sheet 2)

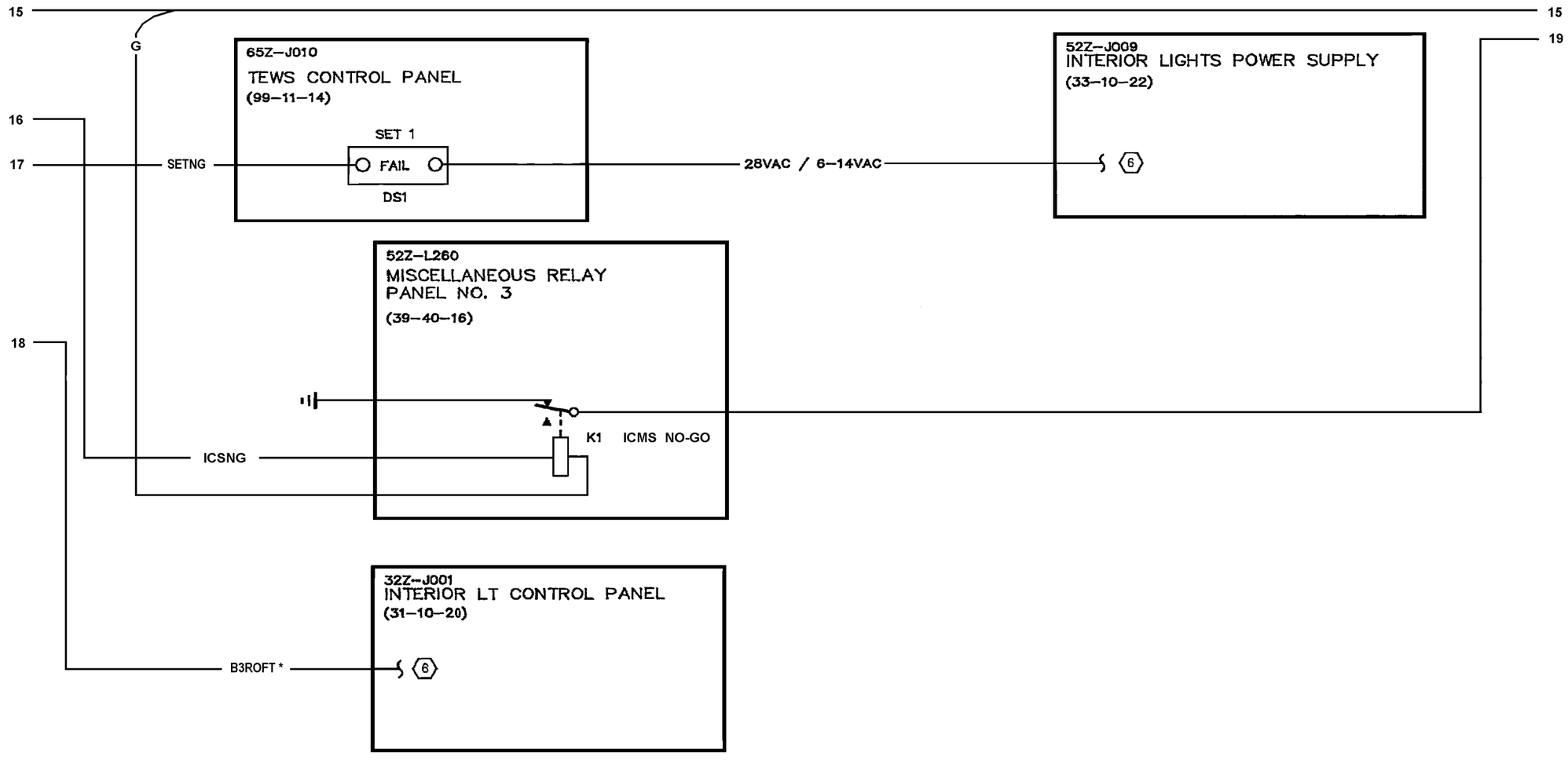

Figure 13-11. ICMS Band 3 BIT Circuit Simplified Schematic (Sheet 3)

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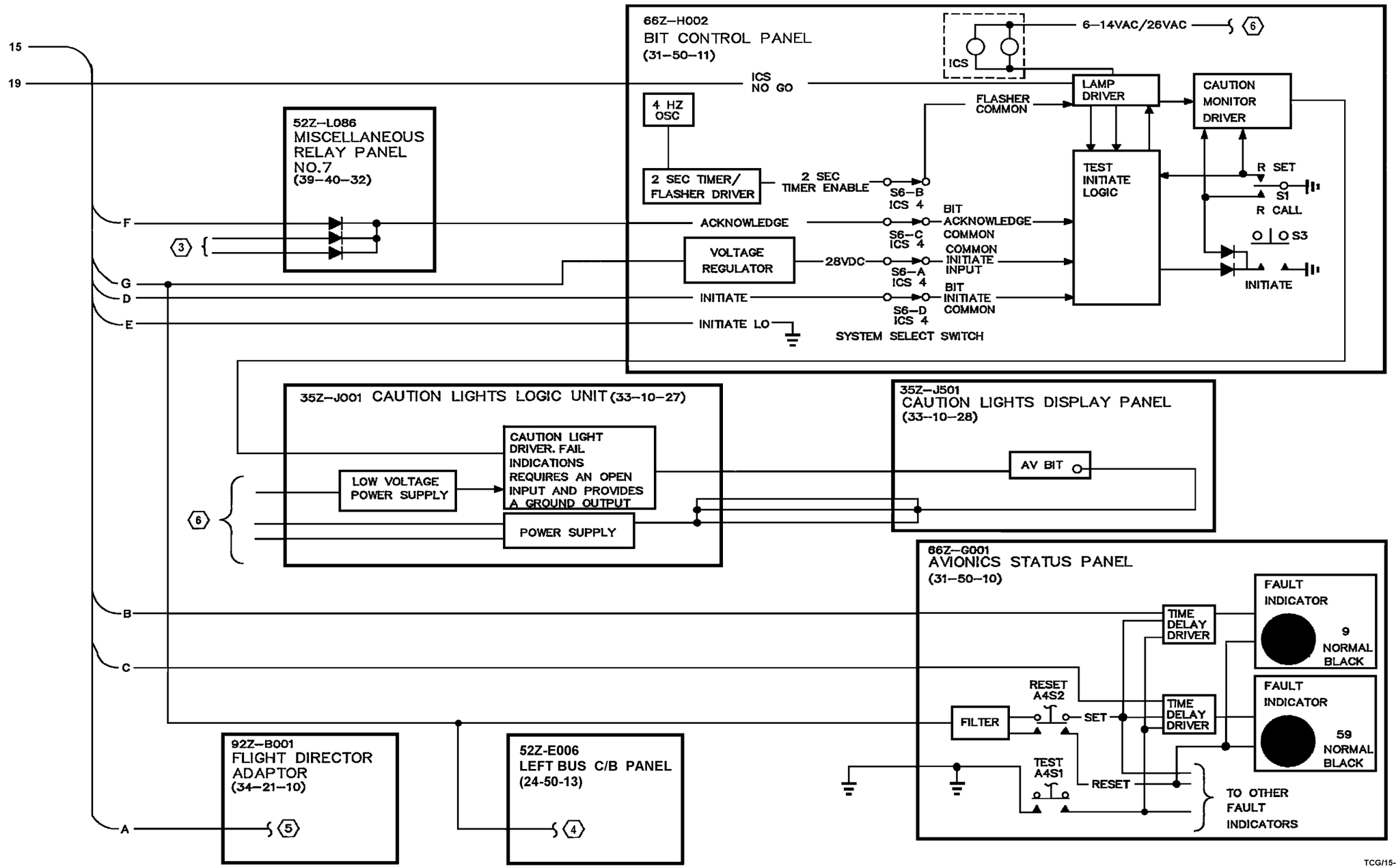

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Figure 13-11. ICMS Band 3 BIT Circuit Simplified Schematic (Sheet 4)

LEGEND

(1) PRIMARY CENTRAL COMPUTER DATA LINES.
(2) SECONDARY CENTRAL COMPUTER DATA LINE.
(3) REFER TO CENTRAL COMPUTER FUNCTIONAL DIAGRAM.
(4) SEE RWR INTERFACE SIMPLIFIED SCHEMATIC.
(5) SEE BAND 3 BIT SIMPLIFIED SCHEMATIC.
(6) REFER TO RADAR SET BLOCK DIAGRAM.

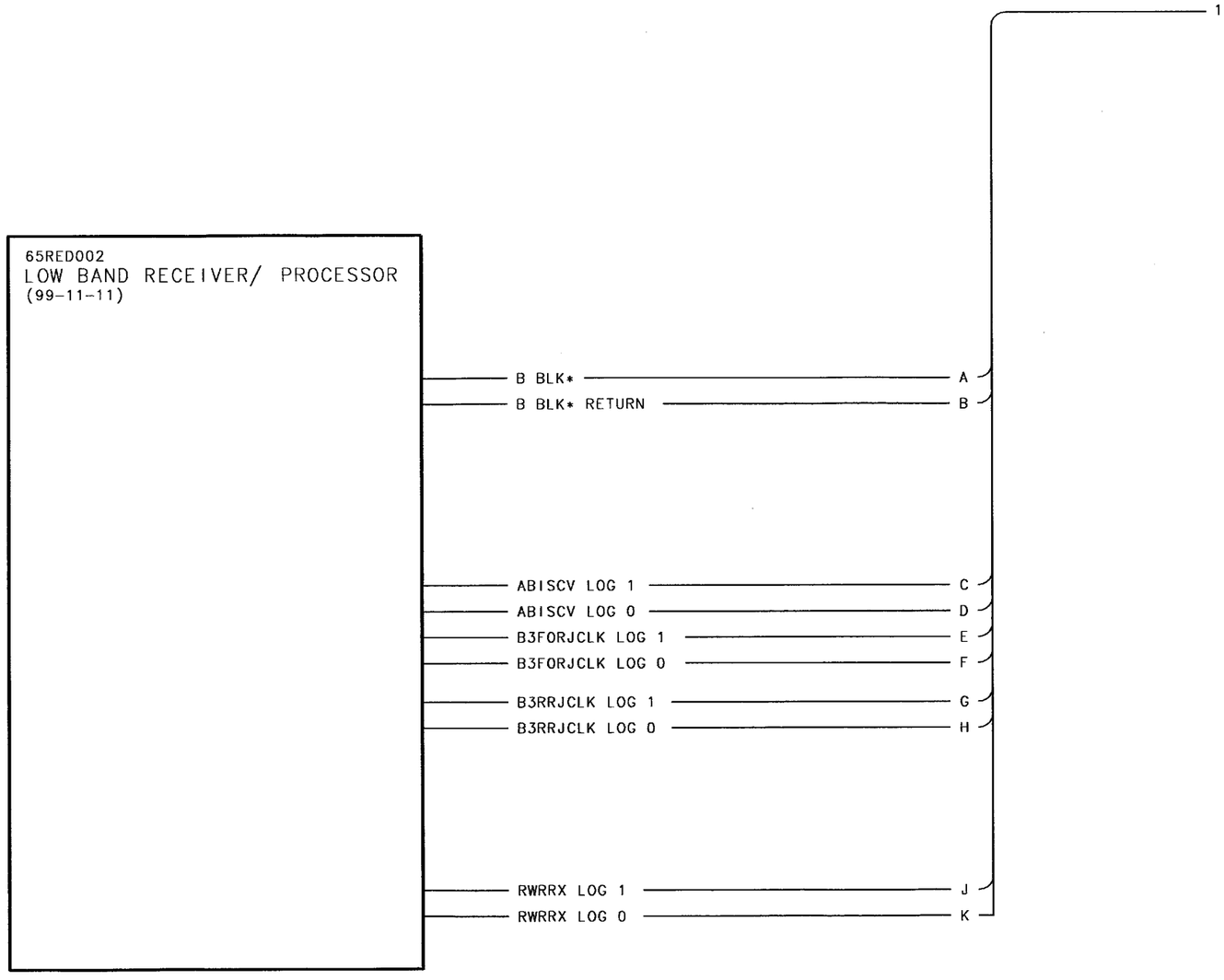

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Figure 13-12. ICMS Band 3 Interface Simplified Schematic (Sheet 1 of 4)

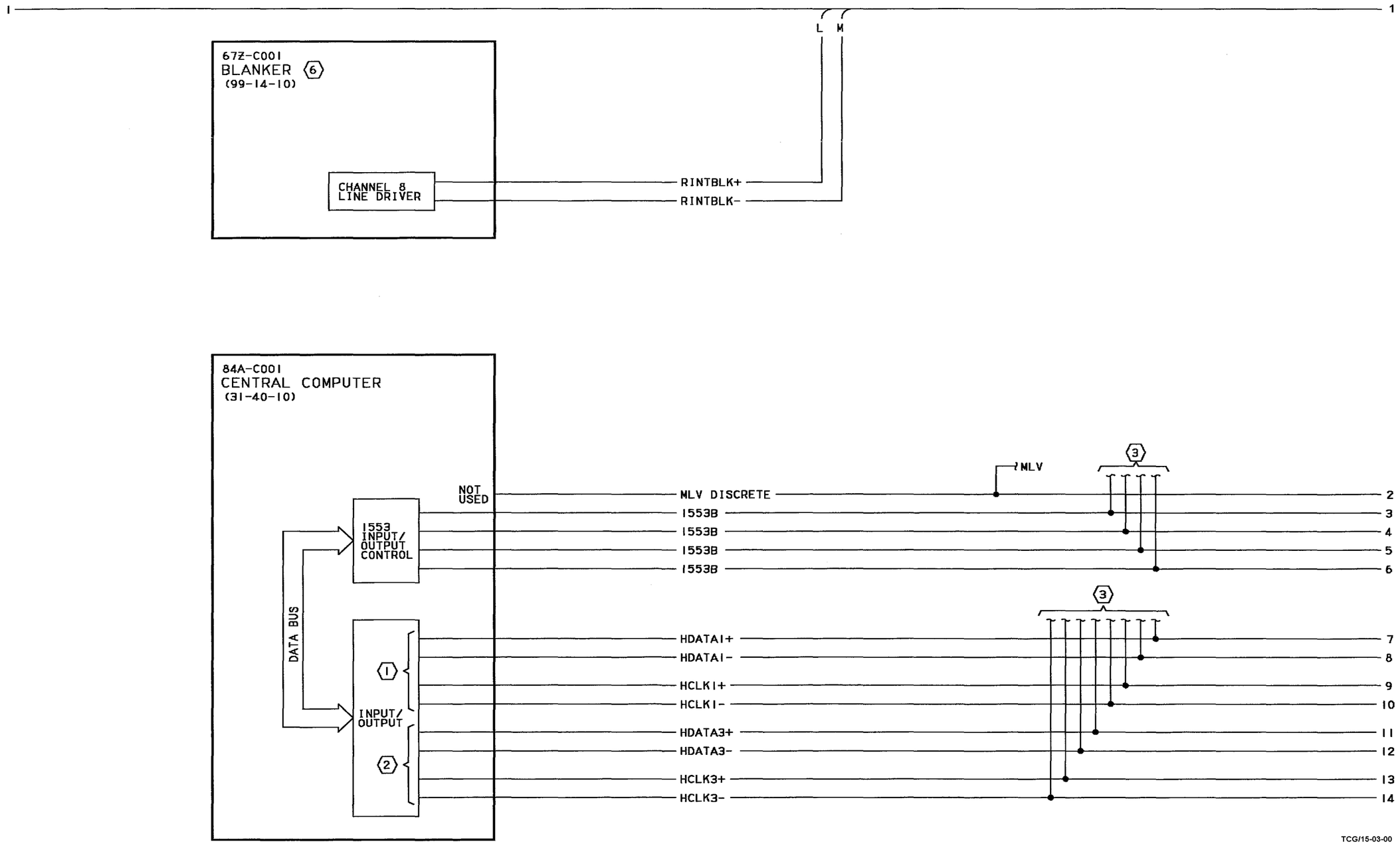

Figure 13-12. ICMS Band 3 Interface Simplified Schematic (Sheet 2)

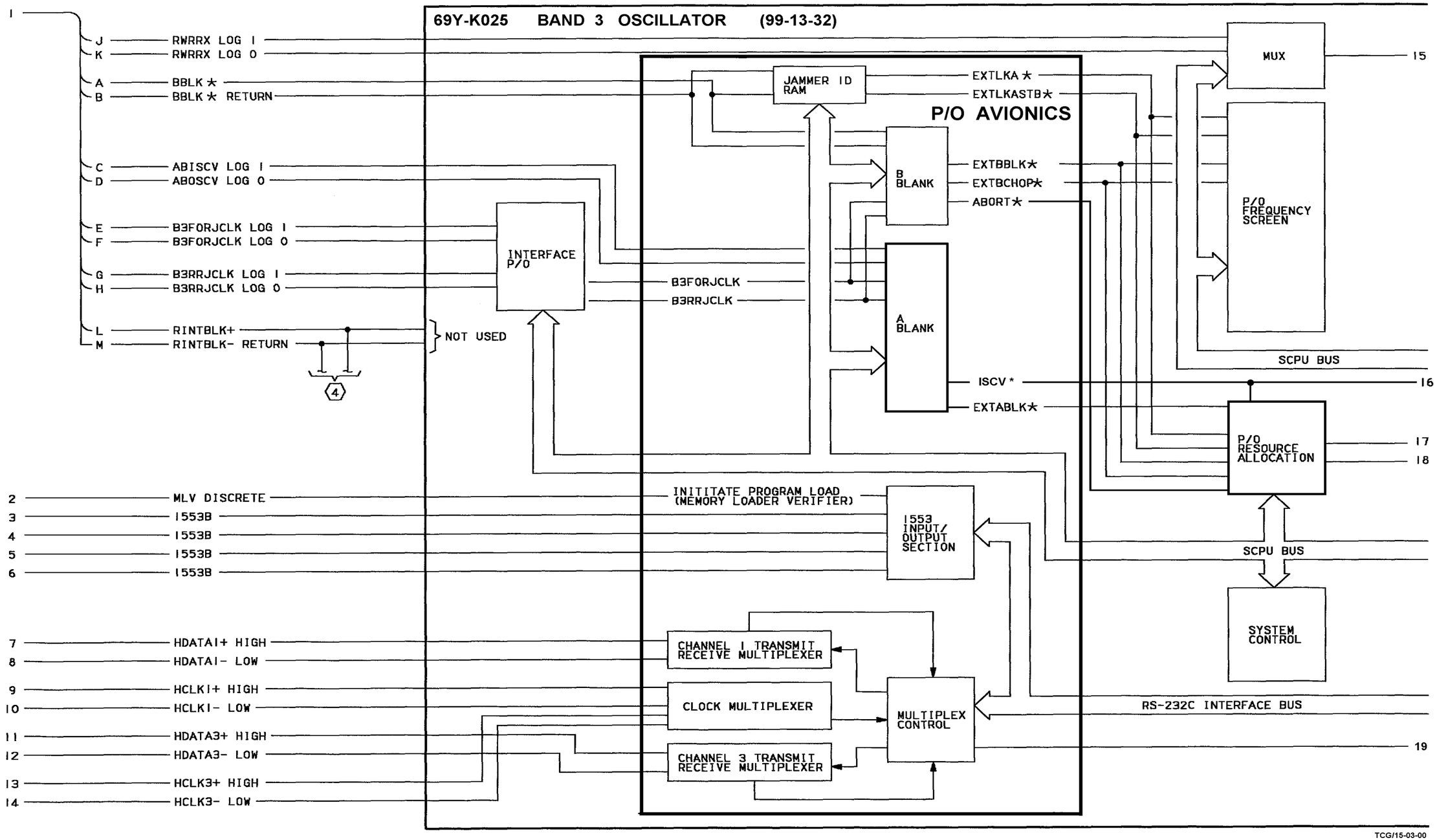

Figure 13-12. ICMS Band 3 Interface Simplified Schematic (Sheet 3)

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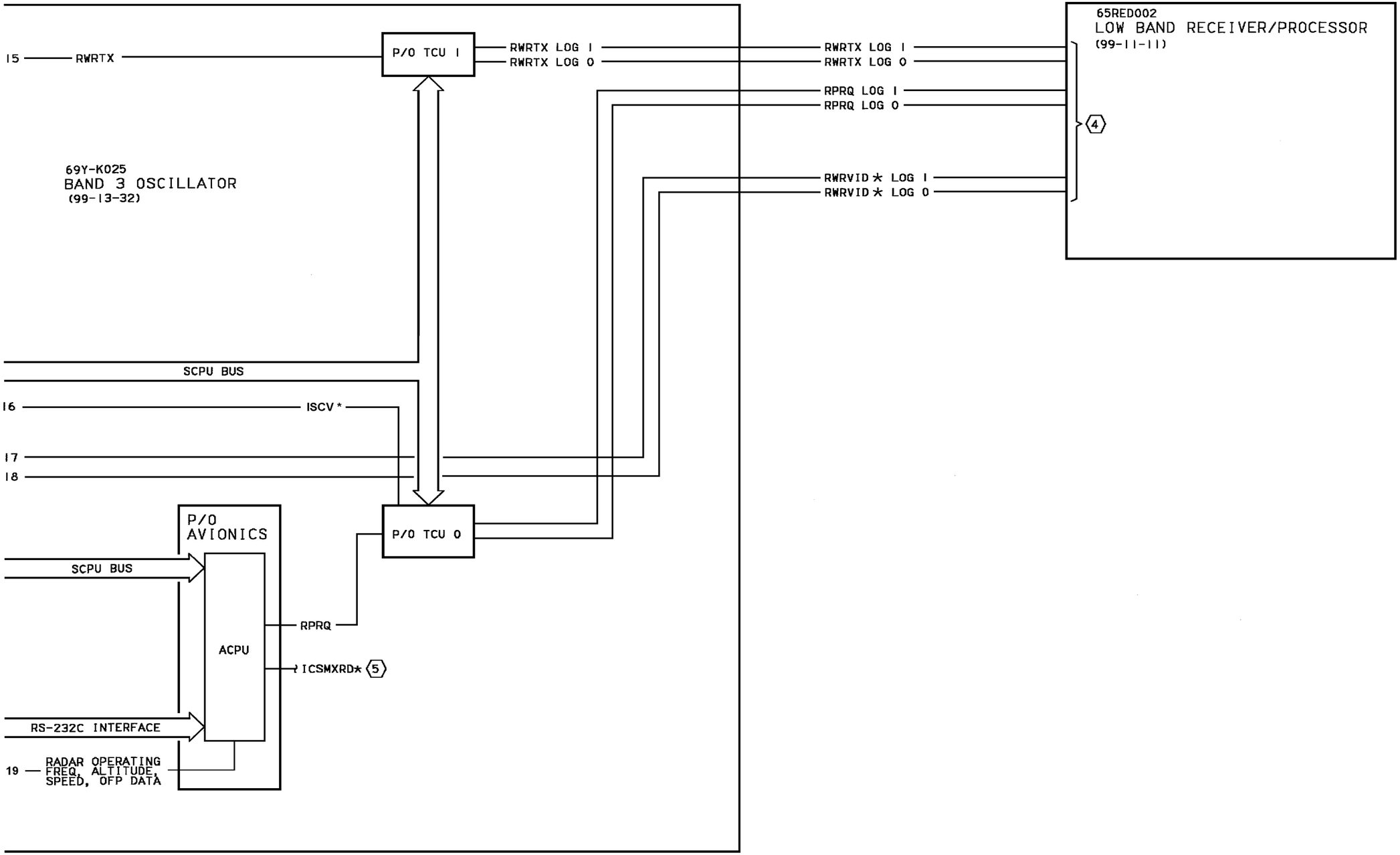

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Figure 13-12. ICMS Band 3 Interface Simplified Schematic (Sheet 4)

RF characteristics with the initial threat data, determines a correction is required in frequency or modulation characteristics, then fine tuning data is sent to the ICMS by way of the data link lines to correct the error. The constant error correction maintains RF signals being radiated by the ICMS while in the auto mode of operation.

13-80. Operation of the ICMS in manual mode is similar to that of auto mode with one exception. The data signals to the tuners are now derived from a programmer located in the respective Set 2 or Set 3 Oscillator.

13-81. **Band 3 Power and Control.** See Figure 13-9.

13-82. The ICMS operates using 115VAC, 3Ø, 400 Hz for primary power and 28VDC for power control. The ICMS power on and mode control is done through controls on the TEWS control panel and TEWS IA control panel. The 28VDC from the 28VDC RDR WRN RCVR PWR circuit breaker 65CBF024 is applied to the ICS relay K1 in the TEWS control panel. A ground is applied to K1 either by the ICS switch being set to OFF or STBY. ICS relay K1 then applies 28VDC to the ICMS cooling control valve and aft ICMS cooling valve. This reduces the ECS cooling air flow to the ICMS. The cooling air flow is reduced to 10 percent of the available ECS cooling air. When the ICS switch is set to the ON, AUTO, or MAN position, K1 deenergizes. This action causes 100 percent of the available ECS cooling air to be supplied to the ICMS. The ICMS cooling control valves operate only when one or both of the aircraft engines are operating. The valve is closed by actuator air pressure (15 PSIG) from the engine bleed air system if either generator stops operating. When operating on ground power, the valves are closed only by external air pressure applied through the ICMS cooling control valve test connector. The ICMS may be operated in standby, manual, or auto mode.

13-83. Standby Mode. The three 115VAC, 3Ø, 400 Hz circuit breakers and the 28VDC circuit breaker to each Band 3 RF Amplifier are applied directly to the EMI filters. The ICS CONT circuit breaker 69CBF021 also supplies 28VDC to the ICS switch on the TEWS control panel. When actuated, the 28VDC is applied through the avionics ground power switching relay to the ICS power relay 69K-L022 in the no. 8 miscellaneous relay panel and the avionics flow control circuit in the avionics air circuit controller. The 28VDC applied to the avionics air circuit controller indicates that more cooling is required. With 28VDC applied, 69K-L022 energizes applying a icson* signal (ground) through the Band 3 Oscillator to enable the auxiliary power supply in the Band 3 RF Amplifier (FWD). Setting the ICS switch on the TEWS IA control panel to STBY routes the return signal (ground) from the avionics circuit in the Band 3 Oscillator to the ICS switch and an open circuit. Therefore, standby mode is selected when the icson* signal is present and the mnlmode and icsauto signals are absent.

13-84. Manual Mode. Manual mode is selected for the ICMS by setting the ICS switch on the TEWS IA control panel to MAN. This action allows the return signal (ground) from the avionics circuit in the Band 3 Oscillator to be applied to the SET-1 switch on the TEWS control panel. Placing the SET-1 switch to MAN causes the Set 1 mode control (manual) ground to be applied to the avionics circuits in the Band 3 Oscillator. The LDG GR relay no. 6 in the Avionics Miscellaneous Modular Relay Panel No. 2 with weight on wheels, applies a gndopinh signal (ground) to the avionics control circuit in the Band 3 Oscillator. This action prevents the ICMS from transmitting in the high power mode with weight on wheels. Manual mode is a stand alone mode.

13-85. Auto Mode. When the SET-1 switch on the TEWS control panel is placed to AUTO, the return signal (ground) is removed from the avionics circuit in the Band 3 Oscillator. This action places the ICMS in auto mode. Placing the COMBAT/TRNG switch on the TEWS IA control panel to TRNG will place the ICMS in the training mode. The LDG GR relay no. 6 in the Avionics Miscellaneous Modular Relay Panel No. 2, with weight on wheels, applies a gndopinh signal (ground) to the avionics control circuit in the Band 3 Oscillator. This prevents the ICMS from transmitting in the high power mode with weight on wheels.

13-86. The Band 3 RF Amplifier (FWD) has three separate power supplies, Auxiliary, HVPS, and LVPS power supply. The 115VAC, 3Ø, 400 Hz and 28VDC primary power is applied to the EMI filters. The input is filtered and applied to the Auxiliary power supply. The 115VAC, 3 Ø, 400 Hz is also applied to the HVPS power supply. An open posid input is applied thru the EMI filter to the auxiliary power supply. Since both the Band 3 RF amplifiers are identical, the posid informs the Band 3 RF Amplifier (FWD) auxiliary power supply which outputs are required at this location in the aircraft. Those added outputs are for the Preamplifier

and the Band 3 Oscillator. In standby with the icson* applied, the auxiliary power supply provides ±16VDC, +170VDC, and +28vdcstby to the EMI filter. The EMI filter supplies ±16VDC and returns to the preamplifier for internal operating voltages. The EMI filter also supplies ±16VDC, +170VDC, and +28vdcstby and returns to the LVPS in the Band 3 Oscillator which outputs the required low voltage (stby) internal voltages. At this time, the Band 3 RF Amplifier auxiliary power supply b3r1icson* signal is sent through the Band 3 Oscillator to the Band 3 RF Amplifier (AFT) auxiliary power supply to initiate standby operation.

13-87. The 115VAC, 3Ø, 400 Hz, 28VDC primary power and icson* applied to the auxiliary power supply produces the reference and housekeeping voltages. The +28vdcstby output is applied to the HVPS and control interface circuits. The 28vdcstby applied to the control interface inhibites the ampbit* and vswrbit* outputs during the warmup period. The pcopgo* enable signal is used to initiate the HVPS processor. This action outputs the 40kHzdr and hvopco* signals to the LVPS. Upon receipt of the hvopco* signal the LVPS applies the 40kHz to the TWT-A and B modulators and low voltage (stby) to all circuits except the RF input. A lver signal (pulse width information) is provided to the HVPS for regulation of the 40kHzdr. The hvlvsk* signal from the HVPS is used to synchronize the LVPS and HVPS to the the switching frequency of the 40 kHz supply. After the output voltages stablizes, a lvpsry signal is applied to the HVPS to start the five-minute warmup period. At this time, the high voltage is applied to the TWT-A and TWT-B.

13-88. After the five-minute warmup, the HVPS supplies the hvwucz* signal to the control interface circuit. This action indicates that the heater voltage for the TWT's has had sufficient time to allow for proper operation. At this time, the ahvry and bhvry signals are applied to the RF power monitor, the control interface circuit and the TWT-A or TWT-B modulators respectively. If the status circuits sense that both the LVPS and HVPS are ready, the HVPS applies the hvlvry* signal to the control interface circuit. The hvlvry* signal allows the control interface, if any faults are present, to set the AMPL BIT indicator DS1 or VSWR fault indicator DS2 respectively. The control interface circuit outputs the iohven* and b3rowucmpl* log 1/0 signals. The iovhen* signal is sent to the HVPS to enable the heater voltage on the high voltage line to the TWT-A and TWT-B. At this time, the moacn* signal from the TWT-A modulator is applied to the HVPS to adjust the helix overcurrent fault trip point. The helix output is applied to the RF power monitor. The b3rowucmpl* log 1/0 signal, indicating warmup complete, is applied to the avionics circuit in the Band 3 Oscillator.

13-89. When all warmup complete signals are received from the Band 3 RF amplifiers, the b3fuop* output initiates full operation of the ICMS. The b3fuop* is applied to the LVPS which outputs the low voltage (OPER) internal voltages for use within the Band 3 Oscillator. The b3uop* is also applied to the LVPS in the Band 3 RF amplifiers (FWD) and (AFT). The LVPS provides the remaining low voltage (OPER) internal voltages necessary for full operation of the respective Band 3 RF Amplifiers.

13-90. During standby (warmup) and operate, the previously mentioned power supplies are monitored for out-of-tolerance conditions and are disabled if a failure occurs. A malfunction within the Band 3 Oscillator LVPS initiates a copsft* output to the EMI filter in the Band 3 RF Amplifier (FWD). The copsft* signal is routed to the auxiliary power supply and starts a shutdown. When the auxiliary power supply receives a copsft* signal or senses an overload in the voltages sent to the Band 3 Oscillator, a b3setcoft* output is sent through the EMI filter to the avionics circuit in the Band 3 Oscillator. If a fault is received by the fault processor circuit, the auxiliary power supply outputs b3r0ft* and ampbit* signals. If a 1vsd* signal is received from the LVPS or an auxiliary power supply fault is detected, a b3r0tempdn* output is enabled. If an overload in the voltages sent to the preamplifier is sensed, a preabitd* output is enabled. The b3r0ft*, b3r0tempdn* and preabitd* outputs are sent to the avionics circuit in the Band 3 Oscillator.

13-91. The Band 3 RF Amplifier (FWD) HVPS receives and provides several fault signals resulting from malfunctions. The vbrsense (bridge voltage regulation sense) output signal is a rectified voltage used by the LVPS to determine if a overvoltage or undervoltage condition exists. The hilntr* (high line transient) signal from the LVPS indicates that the line voltage has exceeded the normal operating range. The HVPS hvpsft output indicates a helix overcurrent fault, cathode undervoltage fault, arc fault, or improper input voltage fault. A thermal sensor on a critical part of the HVPS frame sends a hvpsot* signal when the

overtemperature condition exists (255°F ±5°F). The hvpsft/hvpsot* signals, when present, are applied to the control interface circuit. The hvpsot* signal will inhibit the iohven* signal, which normally enables the HVPS, except during an emergency. The LVPS lvsd*, ampbit*, and b3r0ft* outputs are produced when an overcurrent malfunction exists. The lvsd* signal informs the auxiliary power supply of the malfunction and starts shutdown.

13-92. The Band 3 RF Amplifier (Aft) has three separate power supplies, an auxiliary, HVPS and LVPS power supply. The 115VAC, 3 Ø, 400 Hz and 28VDC primary power is applied to the EMI filters. The input is filtered and applied to the auxiliary power supply. The 115VAC, 3 Ø, 400 Hz is also applied to the HVPS power supply. An grounded posid input is applied thru the EMI filter to the auxiliary power supply. Since both the Band 3 RF amplifiers are identical, the posid signal informs the Band 3 RF Amplifier (Aft) Auxiliary Power Supply not to provide the outputs for the Preamplifier and the Band 3 Oscillator. The 115VAC, 3 Ø, 400 Hz, 28VDC primary power and b3rlicson* applied to the Auxiliary Power Supply produces the reference and housekeeping voltages. The +28vdcstby output is applied to the HVPS and control interface circuits. The 28vdcstby was applied to the control interface circuit inhibiting the ampbit* and vswrbit* outputs during the warmup period. The pcopgo* enable signal is used to initiate the HVPS processor. This action outputs the 40kHzdr and hvopco* output signals to the LVPS. Upon receipt of the hvopco* signal, the LVPS applies the 40kHz to the TWT-A and B modulators and low voltage (stby) to all circuits except the RF input. A lver signal (pulse width information) is provided to the HVPS for regulation of the 40kHzdr. The hvlvsk* signal from the HVPS is used to synchronize the LVPS and HVPS to the switching frequency of the 40 KHz supply. After the output voltages stablizes, a lvpsry signal is applied to the HVPS to start the five-minute warmup period. At this time, the heater voltage on the high voltage line is applied to the TWT-A and TWT-B.

13-93. After the five-minute warmup, the HVPS supplies the hvwucz* signal to the control interface circuit. This action indicates that the heater voltage for the TWT's has had sufficient time to allow for proper operation. At this time, the ahvry and bhvry signals are applied to the RF Power Monitor, the control interface circuit and the TWT-A or TWT-B modulators respectively. If the status circuits sense that both the LVPS and HVPS are ready, the HVPS applies the hvlvry* signal to the control interface circuit. The control interface circuit outputs the iohven* and b3r1wucmpl* log 1/0 signals. The iovhen* signal is sent to the HVPS to enable the high voltage to the TWT-A and TWT-B. At this time, the moacn* signal from the TWT-A modulator is applied to the HVPS to adjust the helix overcurrent fault trip point. The helix output is applied to the RF power monitor. The b3r1wucmpl* log 1/0 signal, indicating warmup complete, is applied to the avionics circuit in the Band 3 Oscillator. When all warmup complete signals are received from the Band 3 RF Amplifiers, b3fuop* output initiates full operation of the Band 3 system. The b3uop* applied to the LVPS provides the remaining low voltage (OPER) internal voltages necessary for full operation.

13-94. During standby (warmup) and operate, the previously mentioned power supplies are monitored for out-of-tolerance conditions and are disabled if a failure occurs. If a fault is received by the fault processor circuit, the Auxiliary Power Supply outputs b3r1ft* and ampbit* signals. If a lvsd* signal is received from the LVPS or an auxiliary power supply fault is detected, a b3r1tempdn* output is enabled. The b3r1ft* and b3r1texnpdn* outputs are sent to the avionics circuit in the Band 3 Oscillator. The Band 3 RF Amplifier (Aft) HVPS receives and provides several fault signals resulting from malfunctions. The vbrsense output signal is a rectified voltage used by the LVPS to determine if a overvoltage or undervoltage condition exists. The hilntr* signal from the LVPS indicates that the line voltage has exceeded the normal operating range. The HVPS hvpsft output indicates a helix overcurrent fault, cathode undervoltage fault, arc fault, or improper input voltage fault. A thermal sensor on a critical part of the HVPS frame sends a hvpsot* signal when the overtemperature condition exists (255°F±5°F). The HVPS hvpsot* output indicates when an overtemperature condition exists. The hvpsft/ hvpsot* signals, when present, are applied to the control interface circuit. The hvpsot* signal will inhibit the iohven* signal which normally enables the HVPS except during an emergency. The LVPS lvsd*, ampbit*, and b3r1ft* outputs are produced when an overcurrent malfunction exists. The lvsd* signal informs the auxiliary power supply of the malfunction and starts shutdown. The b3r1ft* output is applied to

the avionics circuit in the Band 3 Oscillator.

13-95. **Band 3 Receive/Transmit.** See Figure 13-10.

13-96. The Band 3 receive/transmit function receives, detects, analyzes, and transmits a threat response. In the Band 3 mode, the RWR threat information can be accessed if internally processed data becomes unreliable. The Preamplifier and Band 3 Oscillator control and process the received threat.

13-97. RF signals received by the right fin, right wing, left fin, and left wing RWR antennas are applied to the High Band Receiver (p/o RWR). These RF signals are split/divided/attenuated and used by both the RWR and the Band 3 systems The Preamplifier receives the initial RF input threat signals and sends it to the Band 3 Oscillator for analysis. After detection and analysis is completed, the Band 3 Oscillator sends a threat response to Band 3 RF Amplifier (FWD) or (Aft) to be transmitted.

13-98. Preamplifier. The preamplifier provides initial system amplification of the received RF threat signals. The preamplifier receives four RF inputs from RWR, and one RF input from Band 3 RF Amplifier (Aft). The antenna input signals from the RWR are applied to the input diplexer for conversion into Band 3 frequency bands. The b3bit rf is received from the Band 3 RF Amplifier (Aft) and applied to the B3 ALC Switch. The b3bit rf signal is used with an automatic leveling control (ALC) to provide a calibrated amplitude source for the bit mode of operation.

13-99. When the preamplifier is in the normal operating mode, RF energy is input from the RWR and applied to the input diplexer. The input diplexer separates each RF signal into Band 3 frequency bands and attenuates the undesired RF energy. The output of the input diplexer is sent to the B3 Switch/Coupler, amplified and applied to the output diplexer. In BIT, the B3 Switch Coupler switches the antenna input signals to a matched load for isolation.

13-100. The b3bit rf signal applied to the B3 ALC Switch provides a fixed amplitude source to the B3 Switch/Coupler uring BIT. The SWB switch in the B3 ALC Switch is controlled by alcon log 1/0 signal from the Band 3 Oscillator. In BIT, a logic high is applied to each switch. A logic low to the switch is normal operating mode.

13-101. The B3 Switch/Coupler injects RF energy into the Band 3 during BIT and provides isolation for the four RF inputs. The RF switches in the B3 Switch/ Coupler are controlled by RF select signals on the switch control bus. A logic high corresponds to normal operating mode. A logic low corresponds to BIT.

13-102. Band 3 Oscillator. The Band 3 Oscillator has input switching, threat data acquisition and control, ATU selection, and output switching. The input switching circuit applies the threat to Band 3 Oscillator. The threat is detected, identified, and measured. A threat response is then sent to the Band 3 RF Amplifiers (FWD) or (Aft) for transmission.

13-103. Input Switching. The RF antenna signals from the output diplexer is applied to the Band 3 Oscillator RF input. The b3rcvr rf is controlled by the RF select signals from the receiver. These signals select which of the receiving antennas threat signal inputs will be used either individually or in combination to produce the b3 rcvr rf or b3 rf from the RF input. The uncombined RF signals are chopped at a 5 Mhz rate. The combined RF signals are phase shifted by rfdphsh* signal to compensate for interferometer effects of the receive antennas and then applied to the RF switch. The RF switch, upon command from the resource management, applies the b3rcvr rf to the receiver and the b3 rf to the RF Power Divider.

13-104. The B3 Power Divider applies the b3 rf to the rtu0 and rtu1. The rtu0 or rtu1 outputs are sent to the rfd output. Two other RF signals to RFD Output are atu 0, and atu 1. The atu 0 and atu 1 are applied from the Band 3 RF amplifiers (FWD) and (Aft). Each of these four inputs can be switched to develop the b3 f rf or b3 a rf jamming signal.

13-105. Threat Data Acquisition and Control. The receiver in the Band 3 Oscillator receives two RF signals. The b3rcvr rf from the RF input is applied to the receiver. The receiver detects, acquires, identifies, and measures the signal. The clt rf signal from the RFD Output is applied to the receiver which sets the receiver on a jamming resource.

13-106. Threat data acquisition starts with the receiver outputting the frequency data using the rcvr threat bus to the frequency screen and signal acquisition circuits. The frequency screen determines whether the receiver data is valid and is to be stored in one of three pairs of data buffers in the signal acquisition circuit.

13-107. If the RWR system, in comparing the sample RF characteristics with the initial threat data, determines a correction is required in frequency or modulation characteristics, then fine tuning data is sent to the Band 3 to correct the error.

13-108. The frequency screen TCU update circuit determines from receiver data whether an update pulse should be applied to one or more of the eight TCU's to update the timing information. When the frequency screen jam word generator circuit has determined from the receiver frequency data that a threat has occurred, it sends a jamwd(0-3) and its strobe jamstb* to resource allocation jam timer circuit.

13-109. The receiver prioritizer in the resource allocation circuit allocates control of the receiver to one of nine input resources. The resources are applied to the resource allocation circuitry where the highest priority gets control with CLT/Normal being the lowest priority.

13-110. The RF Amplifier prioritizer allocates control of the Band 3 RF Amplifiers (FWD) or (Aft) to one of the competing ATU or RTU requests. There are four tuning units; two agile units atu0 and atu1 and two repeaters rtu0 and rtu1. The tuning unit with the highest priority and active request from the RTU or ATU prioritizer will get control of the selected RF Amplifier.

13-111. ATU Selection. The ATU prioritizer decides which of 17 resources will have control of the ATU in Band 3 RF Amplifiers (FWD) or (Aft). The priority resources are eight jam scenarios, eight TCU's and CI. First priority control is atu0 in Band 3 RF Amplifier (FWD) and second priority is atul in Band 3 RF Amplifier (Aft). The ATU prioritizer decides which ATU has the highest priority. When the controlling resource is decided, the atulkhz, stoops or atulps (5-0), and atu0am or atu1am (1,0) data is applied to the interface or resource management and converted to differential signals and sent to Band 3 RF Amplifiers (FWD) or (Aft).

13-112. The ATU transmitter in the resource management provides a communication interface over the SCPU Bus between the System Control and the ATU's in the Band 3 RF amplifiers (FWD) and (Aft). The RF Amplifier fast data signals are applied to each RF Amplifier. These signals consist of 26-bit words, provide threat characteristics memory concerning frequency, modulation, power levels, as well as CLT. This data is latched to the forward and aft ATU's by the fast data clock signals. Both signals are active simultaneously but only the fast data clock signal to the ATU which has been selected is enabled during transmission. The data rcvd input signals from each RF Amplifier indicates that the fast data was received correctly.

13-113. The threat memory and modulation in the Band 3 RF Amplifiers ATU's receive inputs from Band 3 Oscillator and digitally controlled oscillator (DCO). It processes these signals to establish control signals used for conditioning AM and FM modulation signals. These modulating signals are used to produce the atu 0 signal out of the DCO and sent back to the Band 3 Control Oscillator RFD Output circuit. There are six ATU program lines that provide selection of 1 to 56 ATU threat programs, one of seven closed loop programs, and a rest frequency which is selected by atu0ps0. The atu0am0 log 1/0 signal selects one of three attenuator levels for the atu 0 output that is sent back to the Band 3 Oscillator RFD output. The ATU 1 KHZ clock pulse synchronizes the background noise between the Band 3 RF Amplifier ATU's.

13-114. The Interface Circuit communicates with the receiver module. The b3chopmd* signal instructs the receiver to go into the chop mode. The b3clt/rcv* input signal to the receiver places the receiver in the RCV position during the acquisition and monitor modes and to the CLT position during a chop mode or the CLT mode. The b3rfs/h* signal places the RF activity detector function on hold during RF transmissions. The vps/h* signal places the video processor function on hold during RF Amplifier transmissions.

13-115. Rtu Selection. The RTU prioritizer gives control of the selected RTU to one of eight resources. The selected resource sends an active request and corresponding data to the RF Amplifier prioritizer circuit. The resource with highest priority gets control of rtu0 and second priority has control of rtul. A selected detinh(0,1)* data signal provides the MU No.1 Interface with correlated range/velocity techniques. On the first MU in 0 pulse, the selected RTU requires a constant request and if it has higher priority or none of the other resources are active, it has control of the RTU. This provides a constant RFA request and if none of the resources have higher priority, then this technique will control the selected RF Amplifier.

13-116. The selected RF Amplifier's TWT modulator is enabled and the RFD Output is then controlled by the muout 0 video pulse. Compatibility may be achieved

by sending the video of this jamming over to the selected RTU.

13-117. Output Switching. Switching of the six inputs to the RFD Output is controlled by atu (0-1) on* and rtu(0-1) on* signals from resource allocation. If rtu(0) on* signal is received as the highest priority as determined by the resource allocation, the rtu 0 input signal will be used for the output jamming signal for the Band 3 RF Amplifier (FWD). The rfdaon* and rfdfon* input signal from the interface determines which jamming signal is to be applied to the Band 3 RF Amplifier (FWD) or (Aft). The signals also are used to chop the jamming signals during chop mode. The atu (0-1) rfasel* or rtu (0-1) rfasel* input signal to BIT/ CLT circuit determines whether the jamming signal will go to Band 3 RF Amplifiers as the jamming output signal or to BIT/CLT circuit during bit checkout/ receiver calibration. The BIT/CLT switch is controlled by the BIT/CLT signal from resource allocation. In RFD input to do a bit routine. In CLT mode, the CLT RF is applied to the receiver.

13-118. Band 3 RF Amplifiers (Fwd) And (Aft). The Band 3 RF amplifiers (FWD) and (Aft) are identical; therefore, only the Band 3 Amplifier (FWD) will be discussed.

13-119. The control interface circuit receives command signals from and communicates status and fault information to the Band 3 Oscillator.

13-120. Final Amplification and Modulation Function. After the HVPS has completed its warmup, the ahvry and bhvry signals are applied to TWT A modulator and TWT B modulators. At this time, the high voltage is applied to TWT A and TWT B. The TWT A and B modulators are also supplied with 40khz signals from the LVPS.

13-121. The RF amplification and modulation function is done using a two channel, high power Amplifier. Medium level RF jamming and control inputs are provided by the Band 3 Oscillator. The modulation commands are sent to the control interface circuits, decoded, and applied to the RF Power Monitor.

13-122. The RF input in the Band 3 RF Amplifier (FWD) provides monitoring, attenuation, and amplification of the b3 f rf jamming signal from the Band 3 Oscillator. The RF input circuit produces the atten rf-a for final amplification by the TWT-A. The attenuation control signal from the RF Power Monitor is applied to the RF input. This signal ensures that the atten rf-a signal will not drive the TWT-A into gain compression which would reduce the efficiency of the TWT.

13-123. The TWT A and B modulators are similar; therefore, only the TWT A modulator will be discussed. The TWT A in the selected RF Amplifier is enabled by the b3r0ae* (FWD) signal. The RF power monitor send the amoecl signal to the TWT A modulator. The amoecl signal controls the modulation mode of the TWT A modulator. This allows the TWT A modulator to provide the necessary information on timing and amplitude to the TWT-A on the MOD BUS A. The timing and amplitude of each signal controls the gain and modulation applied to the TWT A.

13-124. The Band 3 RF Amplifier (FWD) has two TWT assemblies each. Both TWT assemblies are similar; therefore, only TWT-A will be discussed. The TWT-A receives the atten rf-a jamming signal from the RF input. The atten rf-a input signal is amplified and modulated to produce the amplified rf-a signal for the waveguide directional coupler.

13-125. The waveguide directional coupler couples the amplified rf-a signal from the TWT-A to the FWD up and FWD down antennas. The output is b3 rf out a. The waveguide directional coupler also provides precision samples of forward power and reverse power to the RF detector. The RF detector uses these signals to calculate the voltage standing wave ratio (VSWR).

13-126. The forward and reverse video signals from the RF detector are used by the RF power monitor to blank any channel which exhibits greater than a predetermined VSWR setting. This is done to protect TWT-A from damage due to excessive reflected power.

13-127. During operation, forward and reverse power delivered to the waveguides/antenna is monitored by the RF input circuit. A sample of the RF jamming signal is detected and compared to a preset threshold reference. The power level sensed is applied to the RF Power Monitor. The signals are sent to the control interface for VSWR analysis. The bittest signal is supplied to enable measurement of the RF during continuous BIT.

13-128. Output Circuits. The b3 rf out a and b3 rf out b from the Band 3 RF Amplifier (FWD) are each applied across two flexible pieces of waveguide to the magic tee. The magic tee distributes the signal through waveguides and Coax Adapter to the Band 3 FWD up

antenna and waveguides to the FWD down antenna. The Band 3 RF Amplifier (Aft) is connected through coax adapters (Pulse/CW) and cable assemblies to the Band 3 Aft antenna.

13-129. **Band 3 BIT Circuits.** See Figure 13-11.

13-130. The built-in test (BIT) routine for the Band 3 enables functional test of the LRUs from end-to-end and provides a visual indication of the equipment status down to the LRU level. Band 3 Oscillator records all BIT failures in a record called BIT LOG. The BIT of the Band 3 is separated into four categories: initialization, continuous, intermittent, and manual initiated BIT.

13-131. The initialization BIT is done when the Band 3 is turned on and weight is off wheels. The BIT includes continuous BIT, LRU tests, and system tests. The BIT routine is completed in less than 1 minute after warm up is complete.

13-132. The continuous BIT circuitry continuously and automatically monitors the RF Amplifiers high voltage arc protection, RWR and Central Computer communication, input prime power, over/ undervoltages, and overcurrent conditions.

13-133. The intermittent BIT routine does system recalibration, monitors continuous BIT, and other initiated BIT test on a periodic basis not to interfere with mission critical functions.

13-134. Manual initiated BIT routine consists of continuous BIT, LRU tests, and system tests independent of the weight-on-wheels indication. Initiated BIT can take up to 10 minutes to complete after initialization BIT and warmup are completed. Initiated BIT routine is enabled only when the Band 3 is in the standby mode. The Band 3 outputs the icsmxrd* signal to the flight director adapter. Upon activating the BIT INITIATE switch on the BIT control panel, the bit initiate signal is applied from the BIT control panel to the bit matrix in the avionics circuit of the Band 3 Oscillator.

13-135. The avionics circuit inputs this data on the SCPU BUS. The system control transmits the control instruction words for the initiated BIT routine. Also, the system control transmits the control instruction word for bit acknowledge, as SCPU BUS output data, to the avionics circuit. The bit matrix, in turn, produces a bit ack signal which is sent to the Miscellaneous Relay Panel No. 7. The Band 3 bit acknowledge signal along with the set2 and set3 bit acknowledge signals are OR'd together. The resultant signal is sent to the Bit Control Panel.

13-136. Band 3 RF Amplifier. The Band 3 RF Amplifiers (FWD) and (Aft) are basically the same except that some of the signals use a 1 instead of a 0. The 0 signifies the forward RF Amplifier and a 1 for the Aft Amplifier. Therefore, only the forward RF Amplifier is discussed.

13-137. RF Amplifier (FWD) monitors input RF power, output forward and reverse RF power, the TWT A and TWT B heater under/overcurrent, TWT A and TWT B overtemperature, TWT A and TWT B modulator overtemperature, HVPS overtemperature, helix overcurrent fault, cathode undervoltage fault, arc fault, or improper input voltage fault.

13-138. The LVPS lvsd*, ampbit*, and b3r0ft* outputs are produced when an overcurrent malfunction exists. The ampbit* output from the LVPS sets the AMP BIT fault indicator DS1. The lvsd* signal informs the auxiliary power supply of the malfunction and initiates shutdown. The b3r0ft* output is applied to the avionics circuit in the Band 3 Oscillator.

13-139. The TWT A and TWT B are similar and so are the TWT A and B modulators. Therefore, only the TWT A and TWT A modulator will be discussed. The TWT A is monitored for traveling wave tube overtemperature. A thermal sensor attached to the TWT initiates a atwot signal when the temperature exceeds the operating range. The atwot signal from the TWT a is sent to the control interface in the event that an overtemperature condition exists. The TWT A modulator is continuously monitored for overvoltage, overcurrent, and overtemperature conditions. When a heater undercurrent condition exists, an ahtui signal is sent to the control interface. When a heater filament overcurrent condition exists, an ahtoi signal is sent to the control interface. Excessive temperature, within the TWT A modulator, causes the amoot* signal to be sent to the control interface. When the duty cycle or pulse width is out of tolerance and the average or burst PRF is in excess of established limits, an amobk fault signal is sent to the control interface.

13-140. The HVPS hvpsft output indicates a helix overcurrent fault, cathode undervoltage fault, arc fault, or improper input voltage fault. The HVPS hvpsot* output indicates when an overtemperature condition exists. The hvpsot* signal will inhibit the iohven*

signal, which normally enables the HVPS, except during an emergency. The hvpsft/hvpsot* signals, when present, are applied to the control interface circuit.

13-141. Critical SRU's in the Band 3 RF Amplifier (FWD) have interlocks. Discontinuity in any of these SRU interlocks causes an INTERLOCK FAULT to be sent to the RF Power Monitor. At selected times during operation, forward and reverse power delivered to the waveguides/antenna is monitored by the RF input circuit. A sample of the RF jamming signal is detected and compared to a preset threshold reference. The power level sensed is applied to the RF Power Monitor. The signals are sent to the control interface for VSWR analysis upon receipt of the bittest signal. The bittest signal is supplied to enable measurement of the RF during continuous BIT.

13-142. If an out of tolerance condition exists, the control interface sends the b3r0fltflg log 1/0 signals to the Band 3 Oscillator. The b3r0pten log 1/0 signals, from the resource management circuit in the Band 3 Oscillator are applied to the RF Power Monitor. The b3r0pten log 1/0 signals are test strobes which produces the indetst signal. The indetst signal strobes the RF input circuit. The b3r0pten log 1/0 signals identify, in conjunction with the extest signal, which RF inputs are to be checked for a no-go or RF power measurement. The extest signal is supplied, when directed by the control interface circuit, during manual initiated BIT. The RF Power Monitor, upon receipt of the extest signal, outputs the resulting inpwrl, afwpwrl, and bfwpwrl signals to the control interface.

13-143. An out of tolerance condition causes the b3r0fltflg log 1/0 signals to be sent from the control interface to the Band 3 Oscillator. The b3r0fltflg log 1/0 signals identify to the avionics circuit in the Band 3 Oscillator that faults exists. Fault identification will be contained in the b3r0cb log 1/0 signals sent to the Band 3 RF Oscillator when requested by the b3r0cb log 1/0 signals. After receipt of the faults, the BIT evaluates whether external threat conditions will permit the BIT to recognize the failures at this time. If external threat environment conditions permit, the BIT sends the info using the b3r0cb log 1/0 signals to the control interface to enable the iohven*, fltord, ampbit*, or vswrbit* outputs.

13-144. The iohven* output will enable the HVPS even if an overtemperature condition exist. The fltord commands the RF power monitor to continue normal operation even if a VSWR or interlock malfunction is detected. If a VSWR out of tolerance condition exists, the Band 3 will operate at a reduced power output. The ampbit* output will set the AMP BIT fault indicator DS1. The vswrbit* output will set the VSWR BIT fault indicator DS2.

13-145. The auxiliary power supply monitors Band 3 Oscillator and preamplifier voltages for overvoltage. The Auxiliary Power Supply senses whether a overcurrent malfunction exists and contains a fault processor circuit to detect faults. A malfunction within the Band 3 Oscillator LVPS initiates a copsft* output to the Auxiliary Power Supply to initiate shutdown. A copsft* or a detected overload in the voltages sent to the Band 3 Oscillator sends a b3setcoft* output to the avionics circuit in the Band 3 Oscillator. If a fault is received by the fault processor circuit, the auxiliary power supply outputs b3r0ft* and ampbit* signals. If a lvsd* signal is received from the LVPS or an auxiliary power supply fault is detected, a b3r0tempdn* output is enabled. If an overload in the voltages sent to the preamplifier is sensed, a preabitd* output is enabled. The b3setcoft, preabitd*, b3r0ft* and b3r0tempdn* outputs are sent to the avionics circuit in the Band 3 Oscillator.

13-146. Band 3 Oscillator. The Band 3 Oscillator controls the BIT. BIT is done by specifically exercising various system functions or hardware circuitry and comparing the results of that testing to known results. The capabilities for failure reporting are an integral part of the OFP.

13-147. The initialize and manual BIT use dedicated bit software to do active tests such as, foundation tests, receiver tests, and end-to-end tests. The foundation test ensure that basic circuitry, communication, controls, and enables are functioning correctly for normal operation of the system. The receiver tests are an intensive validation of the receiver's operational capabilities when subject to various threat types. End-to-end testing is done where selected resources work together to produce actual jamming responses. The entire Band 3 is exercised during BIT to verify jamming techniques.

13-148. Most of the normal tasks done by the OFP software will report operational failures to BIT as a regular part of their operation. BIT will then determine if the failure should be reported to the OFP. This type of failure reporting, along with hardware implemented failure monitoring, is continuous BIT.

13-149. At regular interval, as controlled by the software, the OFP will poll various hardware and software capabilities for operational status. A brief test may be ran or only hardware enabled status bits may be checked. This type of fault monitoring is called intermittent BIT.

13-150. Data instructions and commands from the system control circuits are sent by way of the SCPU BUS to the resource management circuits. The resource management circuits produces b2r0pten and b3r1pten log 1/0 signals. b2r0pten and b3r1pten log 1/0 signals are sent to the RF power monitor circuits in the Band 3 RF amplifiers. The b3r0pten and b3r1pten test enable strobes initiate the RF power measurements or RF input no-go test.

13-151. The system control commands the resource management to check the fault identification of the Band 3 RF Amplifiers and Oscillator. The resource management circuit checks the fault identification of the Band 3 RF Amplifiers using the b3r0cb log 1/0 or b3r1cb 1/0 control buses. The Band 3 RF Amplifiers send the fault identification reply over the b3r0rb log 1/0 or b3r1rb log 1/0 reply buses. The reply is used by the Band 3 Oscillator to determine if Amp Bit or VSWR Bit fault indicator on the respected amplifier should be set. The system control also will send b3scpubit no go fault signal, when applicable, to the bit matrix by way of the SCPU.

13-152. In manual or initialization BIT, there are two checks that are done. The oscillator check is used to insure the Band 3 Oscillator is generating threats correctly. In the oscillator check, a RF signal is produced by atu 1 in the B3 RF Amplifier (Aft). The ATU signal is converted to a digital signal. The digital signal is compared to the original signal.

13-153. The checkout of the B3 Oscillator is started when the system control sends instructions to the resource allocation circuits. The resource allocation produces BIT/CLT signal. The BIT/CLT signal is applied to the BIT/CLT switch inside the resource management circuits (see Figure 13-10). The system control also sends OFP data concerning the characteristics of the bit rf signal to the resource allocation. The resource allocation decodes the information and sends it out as atu1ps(0-5), and atu1am(0-1). The atu1ps(0-5), signals are six ATU. program lines that provide selection of 1 to 56 ATU threat programs, one of seven closed loop programs, and a rest frequency which is selected by atu1ps0. The atu1am0 and atu1am1 signals select one of three attenuator levels for the atu 1 RF output that is sent back to the Band 3 Oscillator RFD Output. These control signals are sent to the interface circuits.

13-154. The interface differentiates the signals and outputs atu1ps(0-5) log 1/0, and atu1am(0-1). log 1/0. These signals are sent to atu 1 in the Band 3 RF Amplifier (Aft). Atu 1 produces the atu 1 signal based upon these signals. Atu 1 signal is applied to the Band 3 ALC Switch in the Preamplifier. The receiver circuits in the Band 3 Oscillator outputs the tupmd* signal to the resource management circuits. Tupmd* sets atucoalc log 1/0 signal high. Atucoalc is applied to the line receiver driver of the B3 ALC Switch. When the atucoalc log 1/0 signal is high, an atu 1 signal is applied to the Band 3 Oscillator. The ATU 1 signal is routed via SWA switch and sent to the RDF Output circuit in the Band 3 Oscillator.

13-155. The ATU signal is applied to the BIT/CLT switch input. The BIT/CLT switch, selects the path for the atu rf signal, clt rf or bit rf. The BIT/CLT signal from the resource allocation circuit places the atu 1 signal on the bit RF line (see Figure 13-10). Bit rf is sent to the RDF Input (see Figure 13-10). In the RDF Input circuits, the bit rf is coupled to the a ant r input line. Bit rf is conditioned by the RDF Input and sent to the receiver circuit as b3rcvr rf. In the receiver circuit, the b3rcr rf signal is digitized and sent to the system control by way of the I/0 bus. The system control transfers the data to frequency screen by way of the scpu bus. The frequency screen compares the signal to the original data from the OFP. If they do not match, the frequency screen produces b3scpubit signal. B3scpubit is sent to the bit matrix.

13-156. The ALC checkout is used to check the Preamplifier, Oscillator, and RF Amplifiers. This check utilizes the same ATU to produce the RF energy as was used in the oscillator checks. The RF signal is sent to the Preamplifier and processed the same as a normal threat signal. Then it is sent to the oscillator. The oscillator digitizes the signal and compares it to the produced RF energy.

13-157. The checkout of the ALC circuits starts in the system control (see Figure 13-10). The OFP data concerning the characteristics of the bit rf energy is sent to the resource allocation circuits from the system control. The generation of the RF energy is done the same as in the oscillator checkout. The RF energy path is changed when the atucoalc signal is set low. The b3

bit rf is routed to the B3 ALC Switch in the Preamplifier. During ALC checkout the resource allocation circuits will output alcon log 1/0 to the line driver of the B3 ALC Switch (see Figure 13-10). Alcon log 1/0 signal sets the switch to the upper position and applies the b3bit rf to the B3 Switch Couplers (see Figure 13-10). B3 bit rf is processed by the Preamplifier the same way as the normal mode of operation. The b3 bit rf is applied to the RDF Input in the Band 3 Oscillator over the f ant r, a ant 1, a ant r, f ant 1 signal lines. The four signals are processed one at a time by the RDF Input. The output of the RDF input is controlled by the RF switch. In this mode, the RF switch outputs the RF signal as b3rcvr rf to the receiver. The receiver digitizes the signal and sends it over the 1/0 bus to the system control. The system control sends the data to the ACPU , by way of the scpu bus. The ACPU compares this data to the OFP data used by the atu 1 to produce the original signal. If the data does not match, the ACPU will produce b3scpubit signal. B3scpubit signal is sent to the bit matrix.

13-158. The bit matrix in the avionics circuits of the Band 3 Oscillator monitors the discrete fault signals produced by the preamplifier, and amplifiers. The bit matrix also monitors the Band 3 Oscillator internally produced fault signals. Upon the receipt of a fault signal, the bit matrix will produce the correct output to initiate an applicable BIT fault indications.

13-159. Fault signals, b3r0ft* and b3r1ft* originate in the RF amplifiers. These signals are identical; therefore, only the b3r0ft* fault signal will be discussed. The bit matrix, upon receipt of the b3r0ft* fault signal from either the auxiliary power supply or the LVPS in the Band 3 RF Amplifier, produces icsng and set1ng. The b3r1ft* will produce an ASP 9 signal. ASP 9 signal is sent from the bit matrix to the Avionics Status Panel. The ASP 9 will set the ASP fault indicator no. 9 (orange).

13-160. Fault signals, b3r0tempdn* and b3r1tempdn*, from each of the RF amplifiers are applied to the bit matrix in the avionics circuits. These signals are identical; therefore, only the b3r0tempdn* fault signal will be discussed. The b3r0tempdn* fault signal originates from the auxiliary power supply in the Band 3 RF Amplifier (FWD). The bit matrix upon receipt of the b3r0tempdn* fault signal produces a icsng fault signal.

13-161. The b3r0wucpl* and b3r1wucmpl*,(warm up complete) status signals from the RF amplifiers are applied to the bit matrix. These signals are identical; therefore, only the b3r0wucmpl* status signal will be discussed. The b3r0wucmpl* status signal is produced by the control interface circuits in the Band 3 RF Amplifier (FWD). The bit matrix upon receipt of the b3r0wucmpl* status signal produces a icsng status signal.

13-162. The b3setcoft* fault signal from in the Auxiliary Power Supply in the Band 3 RF Amplifier (FWD) is applied to the bit matrix. The bit matrix, upon receipt of the b3setcoft* fault signal, produces icsng and set1ng fault signals. The b3setcoft* fault signal sets the C/O BIT DS1 fault indicator (black and white) on the Band 3 Oscillator. The b3setcoft* fault signal also sets the ASP fault indicator no. 59 (orange) on the Avionics Status Panel.

13-163. The b31vpstherdn* fault signal, from the LVPS in the Band 3 Oscillator, is applied to the bit matrix. The b3lvpstherdn* fault signal identifies a fault exist in the LVPS of the Band 3 Oscillator. In the bit matrix, b3lvpstherdn* produces icsng and set1ng fault signals.

13-164. The b3scpubit no go fault signal is applied to the bit matrix by the SCPU BUS. The b3scpubit no go signal identifies that the Band 3 Oscillator is failing BIT. In the bit matrix the b3scpubit no go signal causes the generation of icsng and set1ng fault signals. The b3sepubit no go fault signal also sets the no. 59 fault indicator (orange) on the Avionics Status Panel. The b3scpubit no go fault signal also sets the C/O BIT DS1 fault indicator (black and white) on the Band 3 Oscillator.

13-165. The preabitd* fault signal originates in the Auxiliary Power Supply of the Band 3 RF Amplifier (FWD) and is applied to the bit matrix. The bit matrix, upon receipt of the preabitd* fault signal, produces the icsng and set1ng fault signals. The bit matrix also sets the P/A BIT DS2 fault indicator (black and white) on the Band 3 Oscillator.

13-166. BIT Fail Indications. The avionics circuit in the Band 3 Oscillator receives fault signal inputs from various circuits during the performance of BIT. The resultant fault signals latch or light the applicable fault indicators and initiates the displays. The fault indicator lights and displays are used to identify the faulty LRU.

13-167. During BIT, the oscillator faults are gated to the bit matrix in the avionics circuits of the Band 3 Oscillator. The BIT matrix enables the Band 3

Oscillator fault indicators (black and white) and the applicable ASP fault indicators to set (orange). The set1ng signal is applied to the SET-1 FAIL indicator in the TEWS control panel. The set1ng lights the SET-1 FAIL indicator DS1.

13-168. The BIT matrix output signal icsng is applied to K1 ICMS no-go relay in the miscellaneous relay panel no. 3 and deenergizes K1, causing the ICS light on the BCP to go out. The ICS no go is applied to the lamp driver which in turn applies the ICS no go to the caution monitor driver. The caution monitor driver applies an open on the ICS no go output. The ICS no go (open) signal is applied to the Caution Lights Logic Unit. The caution light driver in the Caution Lights Logic Unit provides a ground output to the caution lights display panel and illuminates the AV BIT light. The icsmxrd* signal indicates the status of the Band 3. When the Band 3 is doing BIT test or during warm-up, the Band 3 sends a low signal (icsmxrd*) to the flight director adapter, indicating that the Band 3 is not ready to transmit or receive data over the 1553 data bus. Upon completion of the warm-up or BIT, the icsmxrd* signal goes high enabling the shift register in the Flight Director Adapter (FDA). The FDA buffers the status signal. The status signal is sent to the Central Computer (CC) to inform that the Band 3 is operational and communication may take place on either the H009 or 1553 bus. The ICS light appears on the BCP to indicate that the ICMS is running BIT.

13-169. Band 3 BIT LOG. Band 3 BIT LOG is a record of faults that have occurred during any of the Band 3 BIT operations. The BIT LOG can be displayed on the MPCD for use in troubleshooting failures that occurred during in-flight or ground operation. Within a BIT LOG there can be more that one BIT run. Each BIT run contains all the failures that occurred. The size of each BIT run is determined by the number of faults that occur during a BIT run. The BIT runs are listed in the BIT LOG in reverse order, the top of the list is the first BIT run. The BIT run located just before the end of BIT LOG marker (FFFF) is the last BIT run. Each BIT run is identified by a start (117A or 117C) and a stop (1156) code. The codes between start and stop identifies the failures that occurred and if any maintenance latches were set.

13-170. The BIT LOG is stored in the ICMS Band 3 control oscillator memory and will retain all failures until the oscillator is reprogrammed or the information is overwritten. On the ground with weight-on-wheels condition, enables the ICMS to send the bit log data to CC for display on the MPCD. If the CC is unable to communicate with the ICMS, ICMS COMMUNICATION FAILURE will be displayed on the MPCD.

13-171. **Band 3 Interface.** See Figure 13-12. The Band 3 Interface receives and distributes inputs from the RWR, Central Computer (CC), Interference Blanker, and radar set.

13-172. RF Compatibility. Operation of the TEWS system depends on exploitation of the radio frequency environment. This environment includes emissions from the radar. The CC provides communication between the TEWS and radar which allows the RWR and ICMS to modify their performance to reduce reception of the radar; allows the CC to show desensitization value of the radar; allows selection of level of RF compatibility to add to the radar modes (offensive), ICMS modes (defensive), or the weapon system modes (auto); and indicate when the ICMS is operating in the radar frequency region.

13-173. Radar/TEWS Interface. The TEWS tries to avoid reception of the radar as much as possible. The Radar/TEWS interface provides radar predicted transmit channels and timing to the RWR on a direct remote terminal to remote terminal transfer. This data is sent to the ICMS by the CC. This data is used by the RWR to establish the frequency screens and by the ICMS to modify or raise receiver thresholds to limit reception of onboard radar transmissions. For those radar modes where the predictions are inaccurate, true frequencies and times are provided to the RWR so processing can prevent detection of the radar.

13-174. Desense Cue. The desense cue provides a performance figure of merit of the radar in A/A Track While Scan (TWS) mode. The radar provides an assessment based on the ratio of the radar measured receiver noise and system thermal noise measurements. This assessment is transmitted to the CC as a percentage of detection range attenuation. The CC converts this percentage into a single digit figure of merit value:

Cue	Value
None	0 to 12.5% degradation
1	12.5 to 37.5% degradation

2	37.5 to 62.5% degradation
3	62.5 to 87.5% degradation
4	87.5 to 100% degradation

The desense cue shows performance desensitization only. The desensitization values may be due to ICMS jamming but may also be external or internal radar noise or system degradation. The CC presents the desense cue as a single digit at the upper left corner of the Avionics Navigation Multiple Indicator (ANMI) or also called the Visual Situation Display (VSD) and is placed outside the radar image grid.

13-175. Priority Control. This provides a means to control the amount of overlap allowed between the radar and ICMS in the frequency region in which both need to operate for full performance. These interference bandwidths are a function of both the ICMS technique category and RF isolation. In TEWS format, pushbutton S4 on the MPCD allows selection to allocate the priority access to frequencies where there is conflict.

- ATAK (Attack/Offensive): The CC uses a special mode that inhibits the ICMS from transmitting in either forward or aft hemispheres over predefined set of frequency regions. ATAK modes restrict the ICMS from operating in the radar region and gives the radar protection from on board transmissions.

- AUTO: The CC calculates forward hemisphere inhibit bandwidths that dynamically adapt to the radar operational modes and operating channels. The bandwidths define a frequency bandwidth to protect the radar performance ability. As the radar mode or weapon mode changes, the CC recalculates inhibit regions and provides this to the ICMS. Radar modes which use frequency agility have wider ICMS inhibit regions to protect the excursion of channels by the radar. Jamming is allowed aft across the entire radar frequency region.

  As the weapon system enters Launch modes, the CC provides a special mode to the ICMS, inhibiting forward and aft transmissions over predefined inhibited bandwidths to be used by the ICMS. After engagement, the CC removes the special mode bit allowing calculated inhibit bandwidths to be used by the ICMS.

  AUTO provides overall weapon system ability, compatible radar protection and increased use of the RF spectrum for ICMS coverage.

- DEFNS (Defensive): The ICMS is unrestricted in RF transmissions. DEFNS gives maximum ICMS RF coverage. If however, the weapon system enters Launch mode, the CC adapts as in AUTO mode. After engagement, the CC removes the special mode bit and returns to the DEFNS configuration.

  In the CC backup mode, the system defaults to DEFNS. The system defaults to AUTO at power up with weight-off-wheels. Power cycles do not affect selection with weight-on-wheels.

13-176. ICMS Conflict Cue. This provides an ICMS cue on the radar display when the ICMS is transmitting forward within the radar ATAK frequency range. This ICMS cue is only in the AUTO and DEFNS modes. If it occurs with a high desensitization value, it could indicate the ICMS is the source of the noise affecting the radar. The ICMS cue is on the radar A/A radar modes at the top left outside the radar image grid. The desense cue, if existing, would be above the ICMS cue.

13-177. Clean/Dirty Channel Logic. When the radar is in TWS and noise is detected, the radar automatically changes to one of the alternate channels trying to move away from the noise and find a clean operating channel.

13-178. RWR. When the ICMS requests data from the RWR, the ACPU in the avionics circuits of the Band 3 Oscillator will output a rprq signal. The rprq output is produced either when program instructions or immediate communications for updating are required. The rprq output, converted by the tcu 0 circuit to a rprq log 1/0 output signal, is sent to the Low Band Receiver/ Processor. The rwrtx log 1/0 signal is used to transmit a data request from the RWR to the ICMS. Rwrtx is applied from the RWR Low Band Receiver/Processor to the mux in the avionics circuits of the Band 3 Oscillator. The rwrtx data is multiplexed and held until the ACPU is ready. The rwrtx data request is then transferred over the SCPU BUS. The transfer of data on the SCPU BUS occurs based on the first-infirst-out principle. To update the RWR, the ACPU sends the requested data consisting of OFP, PFM, patch number, and threat data to the mux using the SCPU BUS. The

rwrtx signal, a response to a data request from the RWR, is sent to TCU 1. The rwrtx signal is converted to a rwrtx log 1/0 signal by the TCU and sent to the Low Band Receiver/Processor.

13-179. Blanking prevents interference between active aircraft systems employing transmitters and receivers. The concept of chop is to line up the forward and aft jam window positions by delaying or phase shifting the aft RF in relation to the forward RF. The bblk* and return is applied from the low band receiver/processor to the jammer ID RAM and BBLANK circuits in the avionics circuits of the Band 3 Oscillator. The BBLANK circuit is used to synchronize blanking. The jammer ID RAM in the Band 3 Oscillator receives the address data from the system control by way of the SCPU BUS. The external look through signal extlka* (0-3) and strobe signal extlkastb* are sent to the resource allocation and frequency screen. Abiscv log 1/0 is applied from the Low Band Receiver/Processor to the ABLANK circuit in the Band 3 Oscillator avionics circuits. Abicsv log 1/0 starts isolation calibration between the RWR and ICMS. The ABLANK circuit is used to synchronize blanking. The b3forjclk and b3rrjclk log 1/0 are applied from the Low Band Receiver/Processor to the Band 3 Oscillator interface circuits. When instructed by the system control, the b3forjclk and b3rrclk are sent to the ABLANK and BBLANK avionics circuits.

13-180. The BBLANK circuit processes the bblk* signal in conjunction with the b3rrjclk signal. The bblk* and b3rrjclk signals are synchronized with the b3forjclk input. The system control instructs the BBLANK circuit to produce either a extbblk* or extbchop* signal, depending on the type of jamming RF used. The extbblk* and extbchop* signals are sent to the frequency screen and to the resource allocation for blanking or chopping the RF Amplifier outputs. The ABLANK circuit processes the abiscv log 1/0 signal in conjunction with the b3rrjclk signal. The abiscv log 1/0 and b3rrjclk signals are synchronized with b3forjclk to provide a extablk* output to the resource allocation circuit. ABLANK also outputs the iscv* signal to the resource allocation and TCU 0 circuits.

13-181. In the resource allocation circuits, iscv* initializes isolation calibration between the Band 3 and the Low Band Receiver/Processor. The resource allocation uses extlka* (0-3)log 1/0 and the related strobes extkastb*, abort*, extablk*, extabblk*, and extbchop* to determine which resource must be prevented from being jammed. The resource allocation circuits outputs rwrvid* log 1/0 to the Low Band Receiver/Processor. The rwrvid* log 1/0 signal identifies jamming that is going to prevent the RWR from receiving actual/true threat data. If incorrect data is sent to the resource allocation circuit, an abort* signal is produced. This abort* signal is sent to the BBLANK circuits and the frequency screen. The abort* signal indicates that the received data instructions are not valid.

13-182. CENTRAL COMPUTER. The Central Computer (CC) 1553 input/output control sends the 1553 B mux bus primary and secondary signals, which are used for transfer of radar operating frequencies, altitude, speed data to the Band 3 Oscillator. The 1553 input/output section of the avionics circuit in the Band 3 Oscillator converts the 1553 B mux bux signals from the CC into RS-232 format. Then, the 1553 B MUX BUS signals are sent to the ACPU on the RS-232 BUS to update the Band 3 data.

13-183. The Central Computer (CC) HOO9 input/output sends hdata 1/3 high/low signal to the channel 1/3 transmit/receive/multiplexer section of the avionics circuits in the Band 3 Oscillator. Hdata 1 or channel 1 data lines are the primary lines and hdata 3 or channel 3 are the secondary lines The channel 1/3 transmit/receive/multiplexer section converts the hdata 1 high/low signal into RS-232 format. The Band 3 also receives channel 1 and 3 clock signals for system timing purposes. The hclk (1,3) high/low is an output from the CC input/output section to the Band 3 Oscillator. The hclk (1,3) high/low signals are applied to the clock multiplexer section of the avionics circuit in the Band 3 Oscillator. The applicable clock signal is sent to the clock multiplexer circuits for input/output control of Band 3/CC data. A synchronization timing signal is derived and sent to the transmit/receive/multiplex circuits for acceptance.

13-184. The CC data is analyzed along with the synchronization timing signal to determine if the CC data is valid. If the CC data is determined to be valid, an enable reply word is sent to the transmit/receive/multiplex circuits to produce a reply word, which is sent to the CC. The CC upon receipt of the reply signal, sends the applicable blanking, OFP and navigational signals. The reply word is sent to inform the CC that

the Band 3 has received valid CC data. The blanking, OFP, and navigation data is placed on the RS-232 BUS for use by the ACPU in the avionics circuits of the Band 3 Oscillator. The ACPU utilizes the information from the RS-232 BUS to update the Band 3.

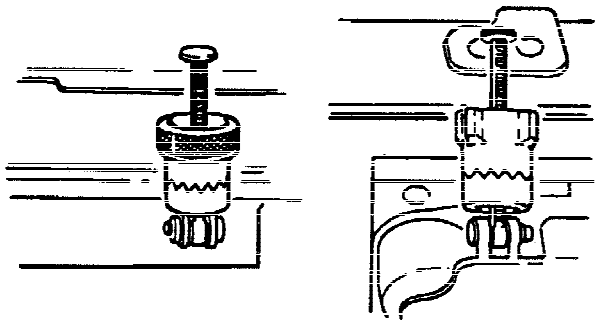
13-185. **SPECIAL MAINTENANCE REQUIREMENTS.**

13-186. **FASTENERS.** Refer to applicable paragraphs below.

13-187. **LRU Spring Lock Fastener Loosening and Tightening.**

CAUTION

To prevent damage to fasteners, do not use hand tools to tighten or loosen knobs.



NOTE

Two types of LRU spring lock fasteners are used. One fastener has a knurled knob and the other a knob with four finger grips.

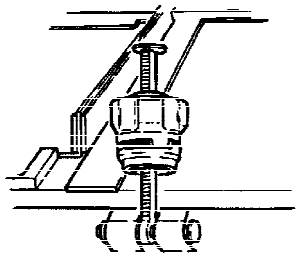
13-188. Loosening.

1. Pull knob out to release serrated collar and turn CCW until knob no longer engages collar when released.
2. Turn knob CCW until collar can be pulled up enough to rotate swivel bolt down to clear mounting foot on LRU.

13-189. Tightening.

1. Rotate swivel bolt up to engage LRU mounting foot.
2. Turn knob CW until knob is tight.
3. Gently rock LRU and turn knob until tight

13-190. **LRU Ratchet Fastener Loosening and Tightening.**



CAUTION

To prevent damage to fasteners, do not use hand tools to tighten or loosen knobs.

13-191. Loosening.

1. Turn knob CCW until swivel bolt can be rotated to clear mounting foot on LRU.

13-192. Tightening.

1. Rotate swivel bolt up to engage LRU mounting foot.
2. Turn knob CW to tighten knob.
3. Gently rock LRU and turn knob until tight.

13-193. **CONSUMABLE MATERIALS LIST.**

13-194. **SUPPLIES (CONSUMABLES).** A list of supplies required to support the organizational maintenance of the ICMS system is provided in Table 13-8.

Table 13-8. Supplies (Consumables)

Nomenclature	Material	Part Number (Mfg Code)
Adhesive		EC1300 (04963)
Brush, Acid Swab		HB643TYPE2 Class 1 Size 1 (81349)
Cleaning Compound		MILC38736 (81349)
Glove, Patient E		MILG36592 (81349)
Lockwire	Monel	MS20995NC20 (96906)
Petrolatum, Technical	Petrolatum	VVP236 (81349)
Tape, Lacing	Nylon	MILT43435TY2-3FNSHE (81349)

13-195. **SUPPORT EQUIPMENT LIST.**

13-196. **TEST EQUIPMENT.** Test equipment required for maintenance of the ICMS system is listed in Table 13-9.

Table 13-9. Test Equipment List

Equipment Number	Nomenclature	Use and Application
AN/ASM-700	Program Loader Verifier Test Set	Refer to 99-13-03, 99-13-05
AN/PSM-37; AN/PSM-6( ) (Alternate)	Multimeter	Trouble analysis
	Goggles, safety	Refer to 99-13-49
MD-3	Trailer, compressed gas air/ nitrogen.	Refer to 99-13-04
PF51-021-1	Hoist, wire rope, radar transmitter	Refer to 99-13-31
68D050112	Kit installation, ICS	Refer to 99-13-31
68D050113	Shield, package ICS	Refer to 99-13-31
68D240021-1001	Adapter, avionics equipment pressure test.	Refer to 99-13-04

SECTION XIV

INTERFERENCE BLANKER

14-1. SYSTEM FUNCTIONAL DESCRIPTION.

14-2. This section contains maintenance instructions for the Interference Blanker MX-9287A, S/S/SN 99-14-10, Reference Designator 67Z-B001.

14-3. **DESCRIPTION.** See Figure 14-1.

14-4. The Blanker prevents interference between active aircraft systems employing radio frequency transmitters and receivers. The Blanker provides blanking pulse outputs for use by associated airborne radio/radar receivers to prevent or reduce electromagnetic interference (EMI) caused by the operation of the associated radio/radar transmitters. The Blanker operates to dispense the blanking pulses received from six source inputs and distributes them to eight predetermined outputs. The Blanker also has expansion capabilities which allow a possible nine inputs and ten outputs. The Blanker also has a built-in test (BIT) capability of monitoring its own operation and alerting the operator of failures within the Blanker.

14-5. Input power requirement for the Blanker consists of 115vac, 400 Hz, single phase aircraft power. Control of the Blanker power is determined by the GND PWR control panel 4 switch position. With the GND PWR control panel 4 switch in the ON position, the Blanker operates from external power. When the aircraft generators come on the line, or external power is removed, the GND PWR control panel 4 switch automatically returns to AUTO. With external power applied to the aircraft and the GND PWR control panel switch in AUTO, no power is applied to the Blanker.

14-6. **PRINCIPLES OF OPERATION.** See Figure 14-2.

14-7. **Input Sensors.** The input sensors receive a blanking pulse from each of the selected systems when the system is transmitting. The blanking pulses are conditioned to provide a logic 1 signal with a pulse width equal to that of the input blanking pulse. The logic 1 output signal from the input sensor is then routed to the output matrix and the BIT circuits.

14-8. **Output Matrix/ Programmer.** The output matrix receives the logic 1 signals from the input sensor, combines them and routes them to the proper line drivers. Distribution of the logic signals may be fixed or programmable.

14-9. Provisions have been made for additional distribution of the logic signals to spare matrix channels.

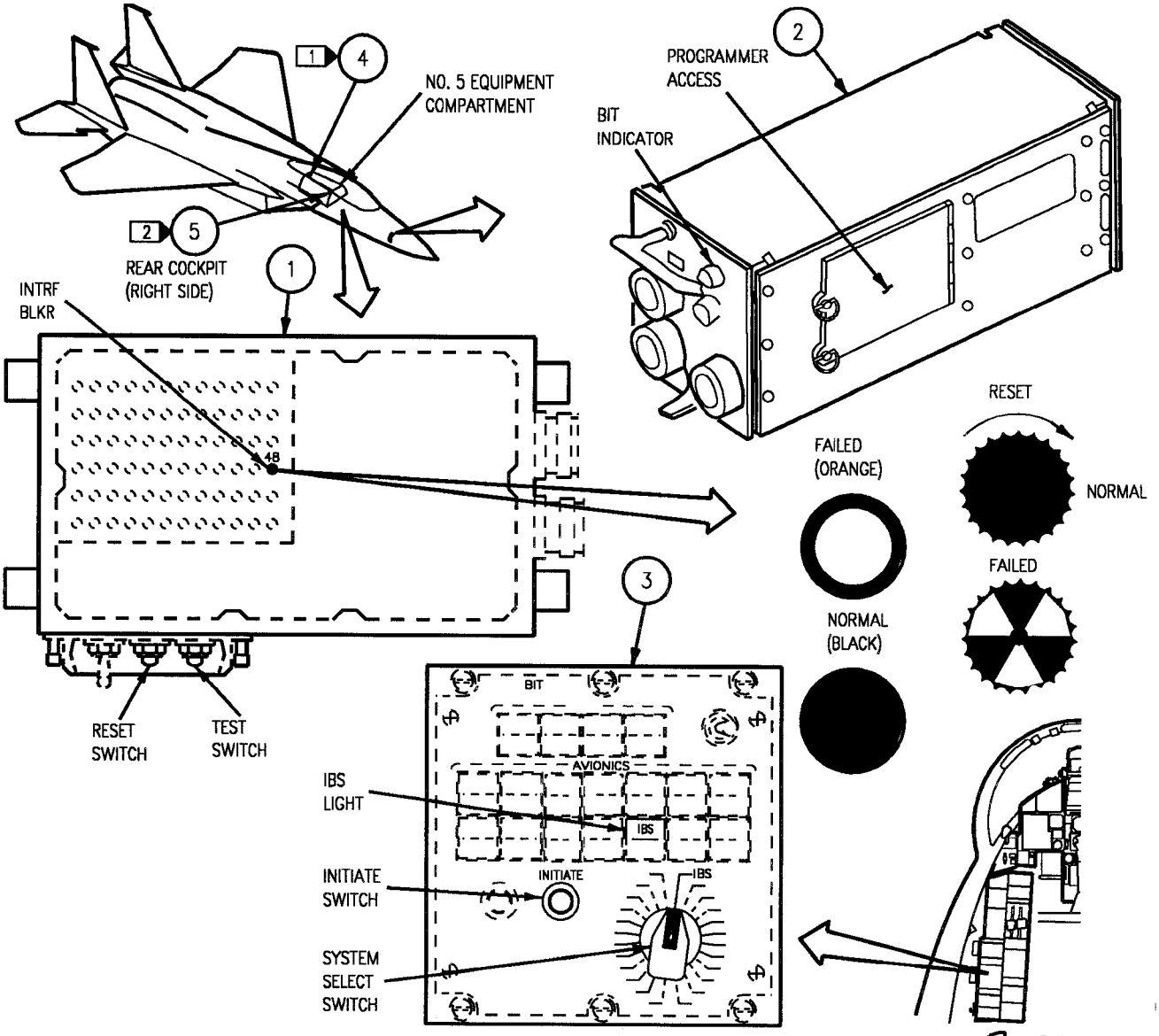
14-10. The programmer, through the use of jumper plugs, inhibits any output derived from any unwanted input from being distributed to the associated line drivers. Only a portion of the available jumper plugs are used at this time. Access to the programmer jumper plugs is provided by a hinged access door secured with two snap fasteners on the side of the Blanker. All jumper plugs are placed in the stored position. This is the normal configuration.

14-11. **Line Drivers.** The line drivers take the logic signals from the output matrix and amplify them to the level required by the particular receiver. A second set of output pulses are sent to the BIT circuits for test purposes. The duration of each channel output equals the duration of the original input pulse. If coincident multiple input pulses occur, the output duration is equal to the time between the leading edge of the first pulse and the trailing edge of the last pulse.

14-12. **Power Supplies.** Two power supplies provide all power used in the Blanker. A continuous monitoring circuit determines proper operation of the power supplies. If any voltage varies more than the nominal value for a predetermined period, either a NO. 1 or NO. 2 FAIL signal is initiated andsent to the NO-GO memory circuits. A NO. 1 FAIL signal is initiated if a high voltage condition occurs on any of the power supply outputs or a NO. 2 FAIL signal is initiated if any low voltage condition exists. The fail-safe circuits provide a power supply inhibit signal, disabling the power supply output if any line driver output pulse duration is greater than a nominal 1.6 second limit.

14-13. **BIT Circuits.** The BIT circuits consist of the continuous BIT, initiated BIT, and fail-safe circuits.

14-14. Continuous BIT. The BIT logic pulses from the line sensors and the BIT logic pulses from the line drivers are compared by the input/output comparator to verify that any output pulse present is coincident with an input pulse. If no output pulse is present coinciding



INDEX NO.	COMMON NAME	S/S/SN	REF DES	ACCESS
3 1	AVIONICS STATUS PANEL	31-50-10	66Z-G001	NOSE WHEELWELL
2	INTERFERENCE BLANKER	99-14-10	67Z-B001	DOOR 3R
3 3	BIT CONTROL PANEL	31-50-11	66Z-H002	COCKPIT
1 3 4	LEFT GND PWR SWITCHING CIRCUIT BREAKER PANEL	24-50-14	52Z-L163	NO. 5 EQUIPMENT COMPARTMENT
2 3 5	MISCELLANEOUS CIRCUIT BREAKER	24-50-15	52Z-K261	REAR COCKPIT (LEFT SIDE)
3 6	GND PWR CONTROL PANEL	39-10-13	52Z-H069	COCKPIT

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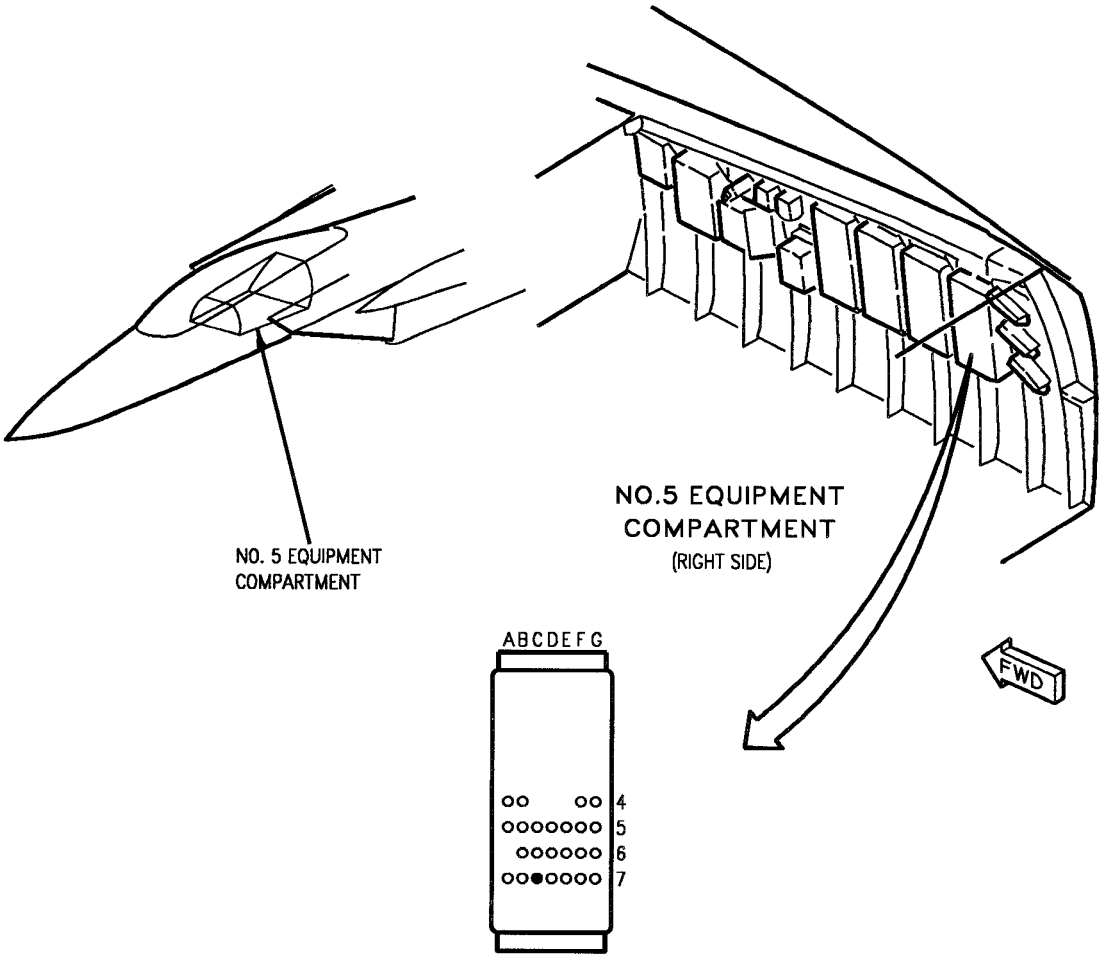
Figure 14-1. Interference Blanker (Sheet 1 of 3)



1 52Z-L163	LEFT GROUND POWER SWITCHING CIRCUIT BREAKER PANEL (24-50-14)		
ZONE	REF DES	NOMENCLATURE	BUS
C7	67CBL002	INTRF BLANKER	L 115VAC ϕC NO. 4

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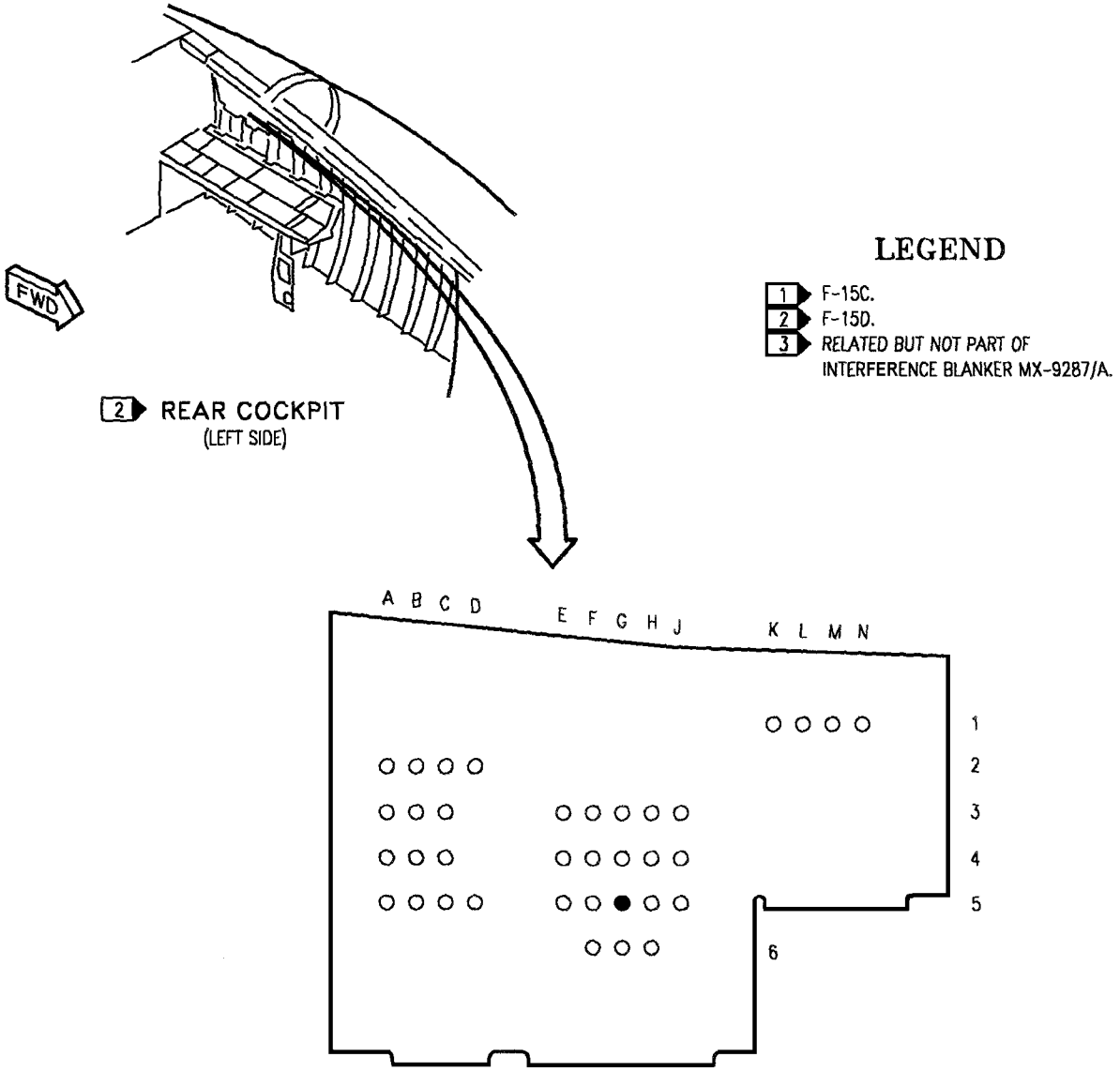
Figure 14-1. Interference Blanker
(Sheet 2)



2 52Z-K261 MISCELLANEOUS CIRCUIT BREAKER/
LEFT GROUND POWER SWITCHING PANEL (24-50-14)

ZONE	REF DES	NOMENCLATURE	BUS
G4	67CBK002	INTERF BLANKER	L 115VAC ϕC NO. 4

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Figure 14-1. Interference Blanker (Sheet 3)

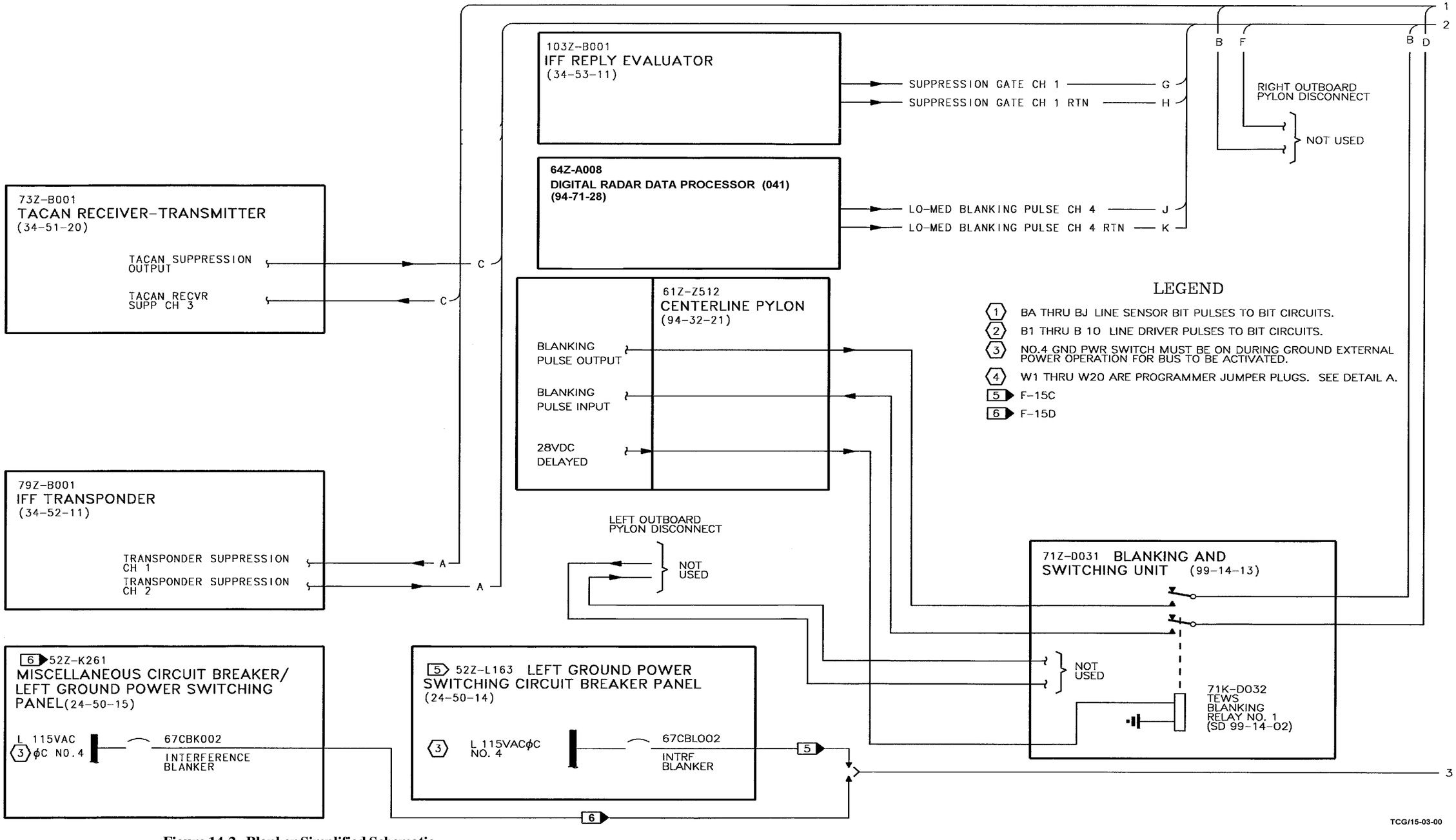

Figure 14-2. Blanker Simplified Schematic (Sheet 1 of 5)

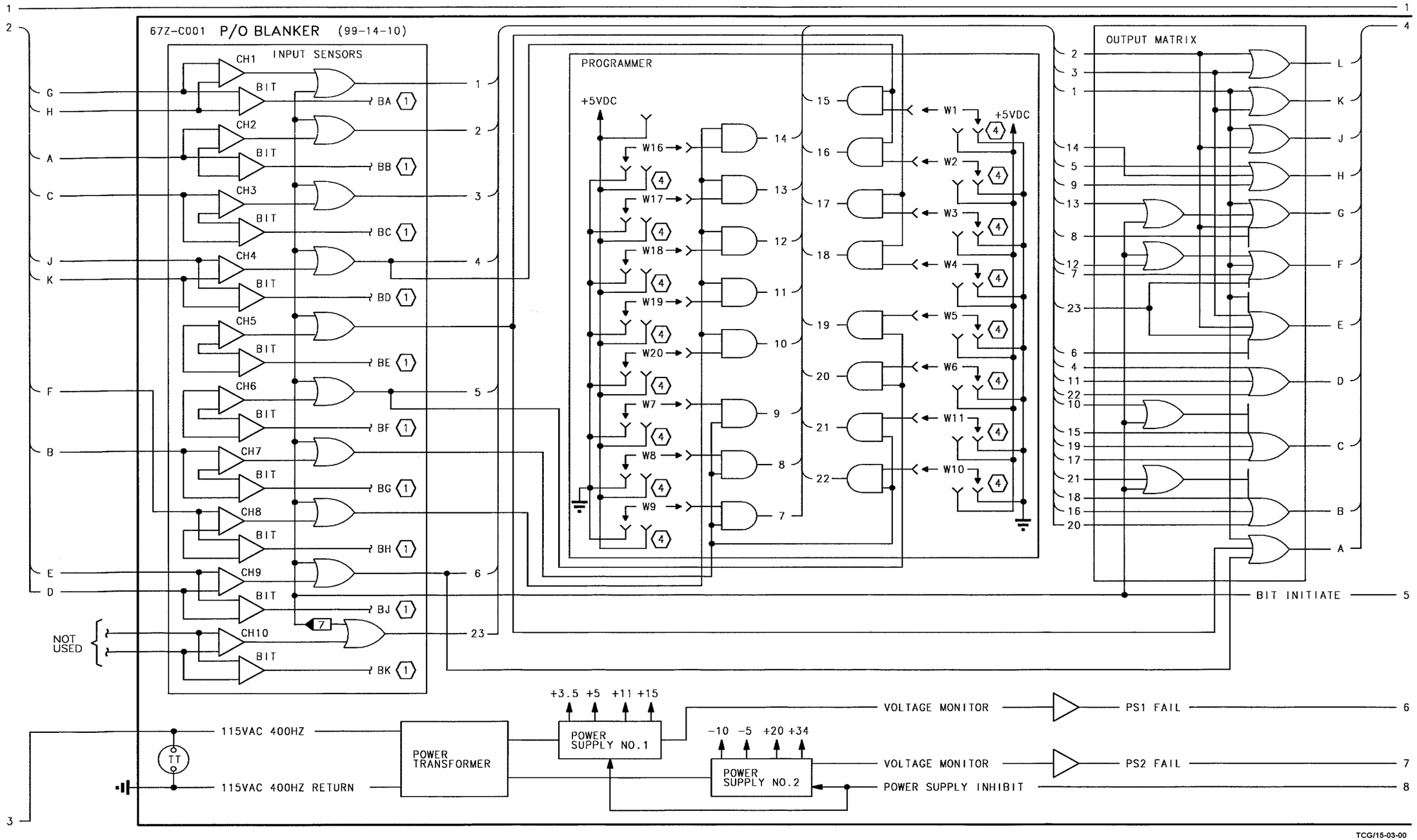

Figure 14-2. Blanker Simplified Schematic (Sheet 2)

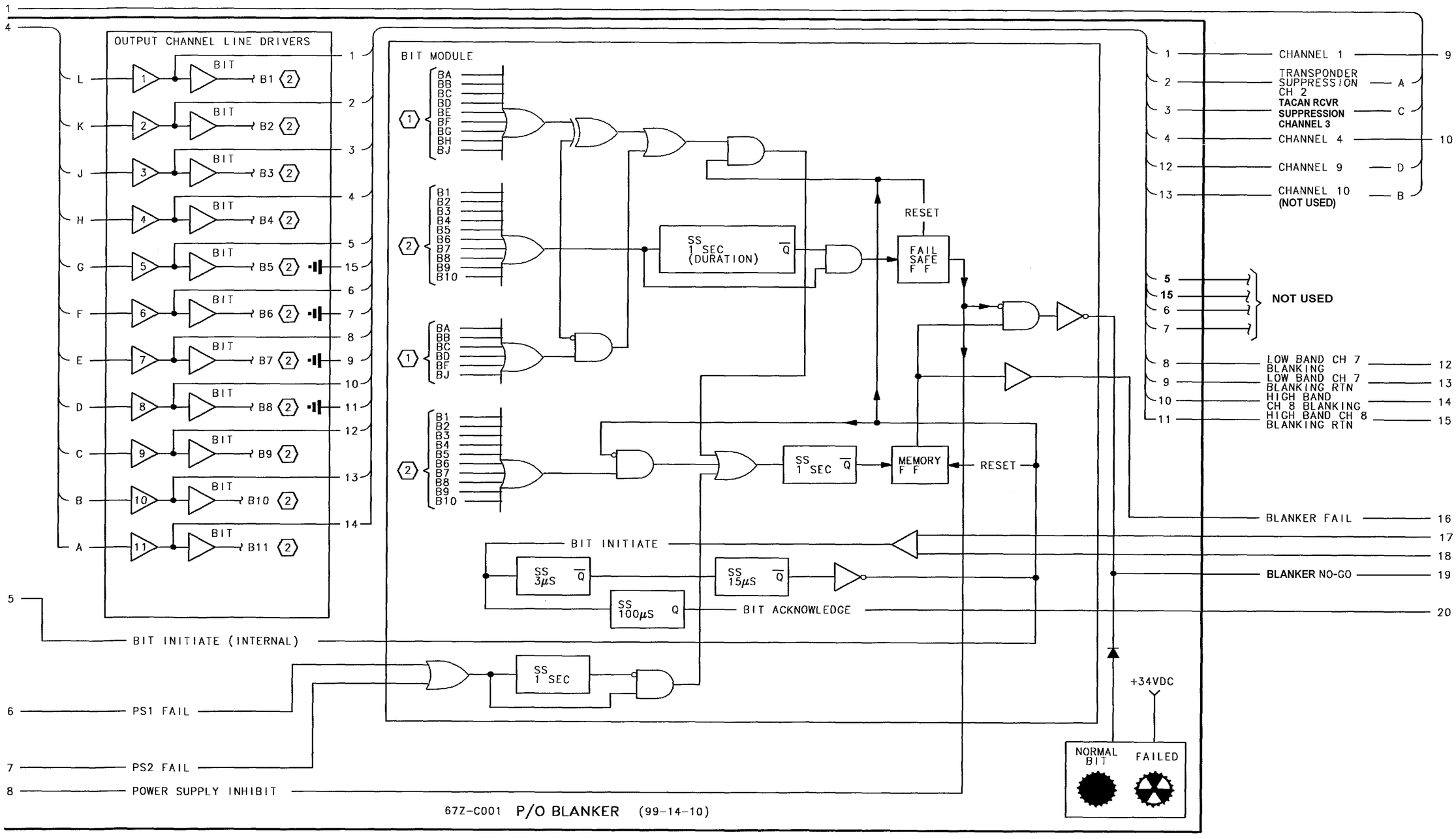

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Figure 14-2. Blanker Simplified Schematic (Sheet 3)

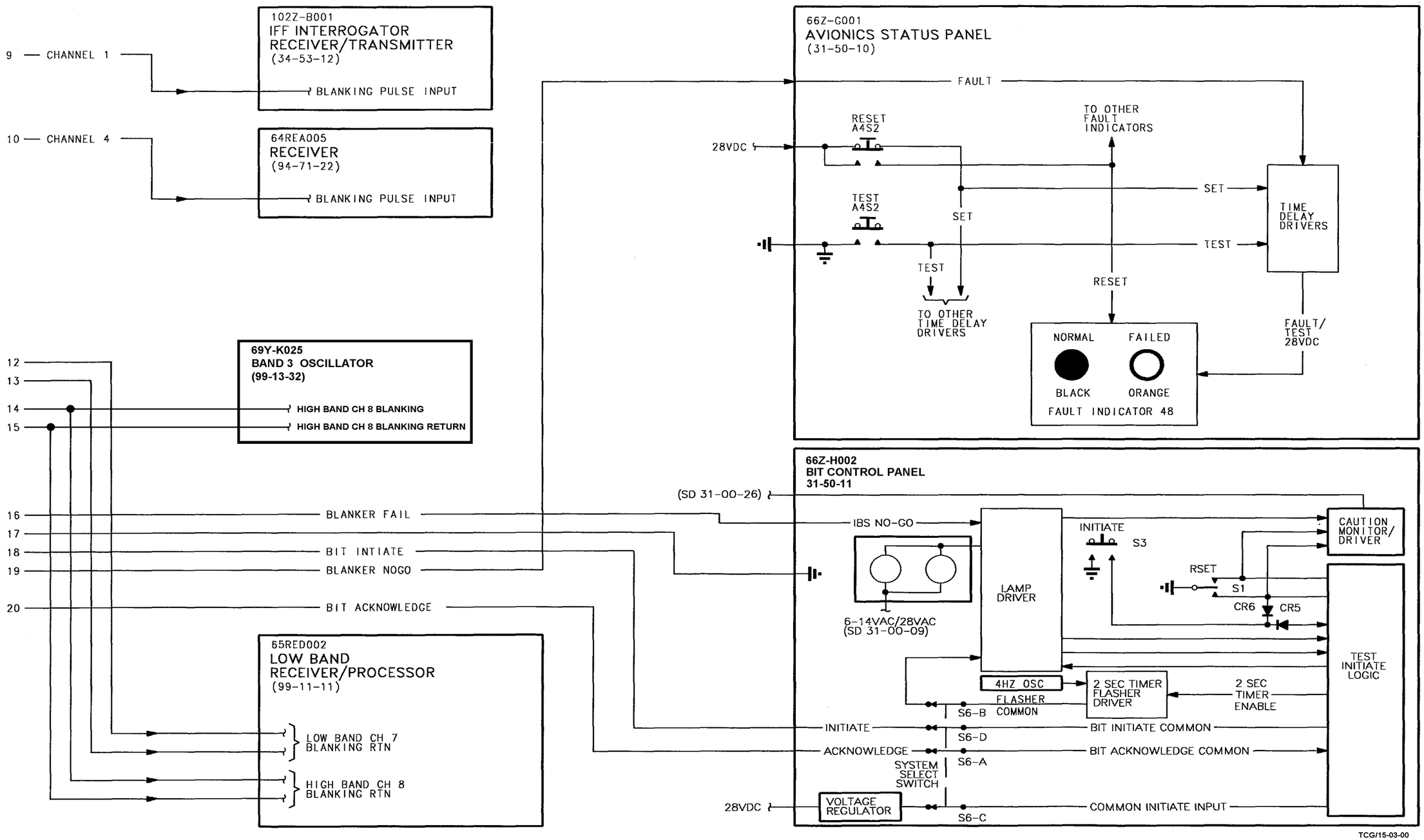
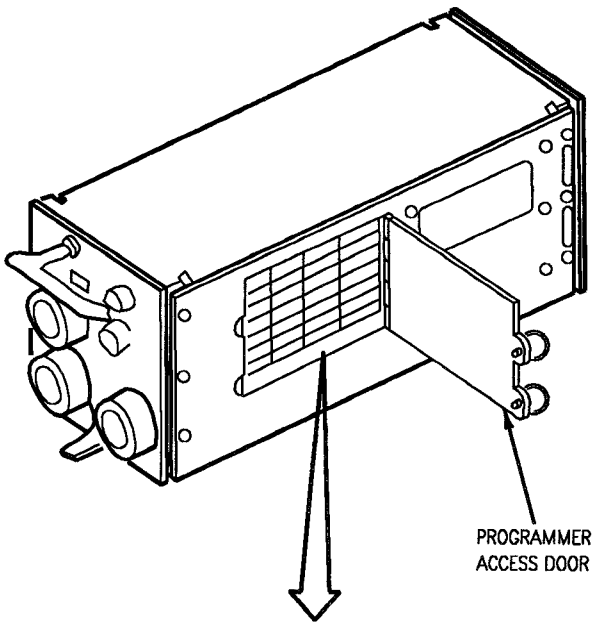
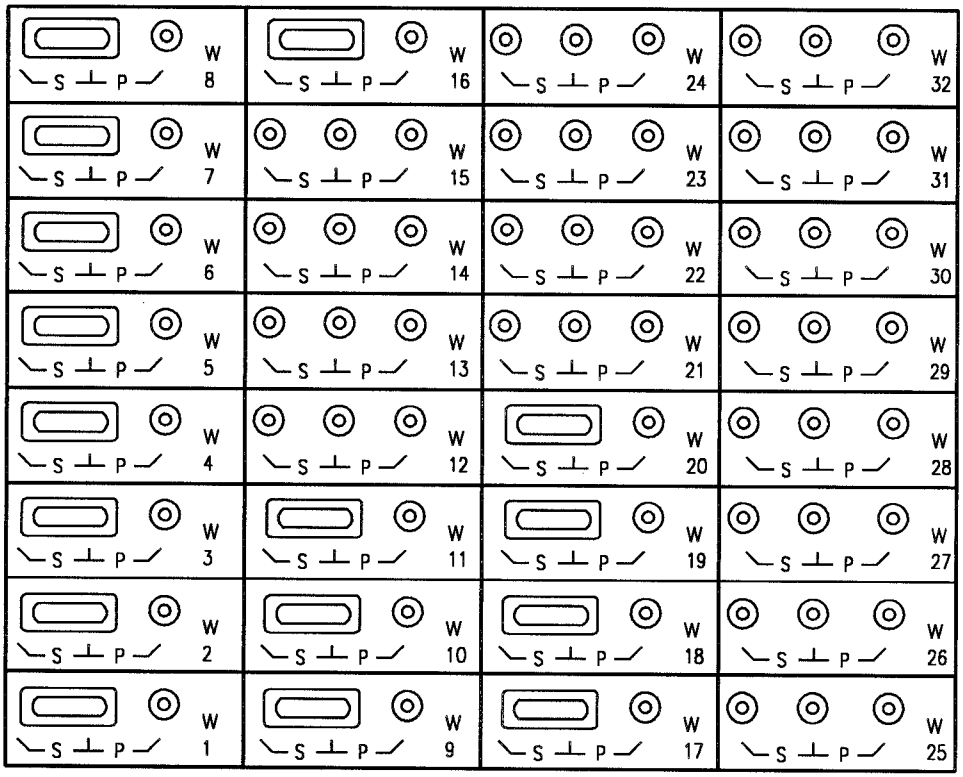


Figure 14-2. Blanker Simplified Schematic (Sheet 4)





PROGRAMMER PANEL

DETAIL A

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Figure 14-2. Blanker Simplified Schematic (Sheet 5)

with an input pulse, the NO-GO memory flip-flop is set, supplying a set NO-GO signal to the BCP IBS light and an LRU-NO-GO signal to the ASP fault indicator 48 and the BIT indicator on the front of the Blanker.

14-15. Initiated BIT. Manual positioning of the system select switch to IBS and actuation of the INITIATE switch on the BCP enables the Blanker BIT circuits. The BCP sends a 20 to 28vdc signal to the initiated BIT circuitry. The initiated BIT circuitry then sends a BIT acknowledge pulse back to the BCP which starts the IBS light flashing for approximately 2 seconds to give a visual indication that the initiated BIT is now being performed. In addition to the BIT acknowledge signal, an internal initiated BIT pulse is generated to provide the below listed functions:

a. Reset the fail-safe and NO-GO memory circuits to a GO condition.

b. Inhibit the input/output continuous BIT comparator.

c. Simultaneously send pulse to all input sensor logic circuits to simulate an input signal on all channels.

d. Enable channels 5, 9 and 10 outputs with the programmer jumper plugs in the stored position.

e. Enable the initiated BIT input/output comparator to verify outputs present on all 8 channels.

14-16. The BCP IBS light flashes for approximately 2 seconds. If no failure in the Blanker is detected, the IBS light remains off. If a failure is detected, the NO-GO memory circuits are initiated to provide a set NO-GO signal to keep the IBS light on and an LRU-NO-GO signal setting the ASP fault indicator 48 to orange and the Blanker BIT fault indicator to a black and white fail indication.

14-17. Resetting of the BIT circuits is accomplished as listed:

a. The IBS light is reset by positioning the RSET/ RCALL switch to RSET and releasing.

b. The ASP fault indicator 48 is reset by pressing the RESET switch on the ASP.

c. The Blanker BIT indicator is reset by manually rotating the BIT indicator CW.

d. The Blanker internal NO-GO memory circuits are reset by positioning the BCP system select switch to IBS and pressing the INITIATE switch.

14-18. Fail-Safe. The fail-safe circuit determines if any line driver output pulses are greater than 1.6 ±0.6 seconds in duration. If any output pulse exceeds 1.6 seconds, a power supply inhibit signal is generated and sent to the power supplies to shut down power to some portions of the Blanker. At the same time, an inhibit signal is sent to the LRU-NO-GO circuits preventing the Blanker BIT fault indicator from setting black and white and fault indicator 48 on the ASP from setting orange. Disabling the power supplies initiates NO. 2 FAIL signal (indication of a low or no voltage) to the NO-GO memory. The NO-GO memory circuits enable an LRU-NO-GO and a SET- NO-GO. The SET-NO-GO lights the IBS light on the BCP; however, the LRU-NO-GO is inhibited by a fail-safe circuit. Since fail-safe condition may have been generated by a one time error of an input, it is possible to do an initiated BIT on the Blanker and clear the fail-safe NO-GO. If an initiated BIT is performed, and the problem no longer exists, the IBS light on the BCP goes off and normal operation resumes.

14-19. **System Interface.** The LRU and associated systems which are interfaced by the Blanker are described in paragraphs 14-20 thru 14-24. Refer to Table 14-2.

14-20. IFF Reply Evaluator. During IFF interrogator transmissions the IFF Reply Evaluator, an LRU of the air-to-air IFF Interrogator System, provides a suppression signal to the Blanker channel 1 line sensor. The Blanker channel 1 line sensor output is applied as listed:

a. Channel 2 line driver which supplies a blanking signal to the IFF transponder, an LRU of the IFF transponder system.

b. Channel 3 line driver supplies blanking signals to the TACAN Receiver/Transmitter Adapter, an LRU of the TACAN System.

c. Channel 7 line driver which supplies a blanking signal to the low band input of the low band receiver/processor, an LRU of the RWR.

14-21. IFF Transponder. When transmitting in reply to interrogations, the IFF transponder, an LRU of the IFF transponder system, provides a suppression signal to

the Blanker channel 2 line sensor. The Blanker channel 2 line sensor output is applied to the below:

a. Channel 1 line driver which supplies a blanking signal to the IFF interrogator receiver-transmitter, an LRU of the air-to-air IFF interrogator system.

b. Channel 3 line driver supplies blanking signals to the TACAN Receiver/Transmitter Adapter, an LRU of the TACAN System.

c. Channel 7 line driver which supplies a blanking signal to the low band input of the low band receiver/processor, an LRU of the RWR.

14-22. TACAN Receiver-Transmitter/Adapter. During TACAN transmissions the TACAN receiver-transmitter/adapter, an LRU of the TACAN system, provides an input pulse to the Blanker channel 3 fine sensor. The Blanker channel 3 line sensor output is applied to the below:

a. Channel 1 line driver which supplies a blanking signal to the IFF interrogator receiver-transmitter, an LRU of the air-to-air IFF interrogator system.

b. Channel 2 line driver which supplies a blanking signal to the IFF transponder, an LRU of the IFF transponder system.

c. Channel 7 line driver which supplies a blanking signal to the low band input of the low band receiver/processor, an LRU of the RWR.

14-23. Radar Data Processor. During radar transmission, the Radar Data Processor, an LRU of the radar system, provides an input pulse to the Blanker channel 4 line sensor. The Blanker channel 4 line sensor output is applied to the below:

a. Channel 8 line driver which supplies a blanking signal to the high band input of the low band receiver/processor, an LRU of the RWR, and Band 3 Oscillator, an LRU of the ICMS.

b. Channel 9 programmer matrix which routes channel 4 line sensor output to channel 9 line driver when programmer jumper plug W1 is in the program (P) position.

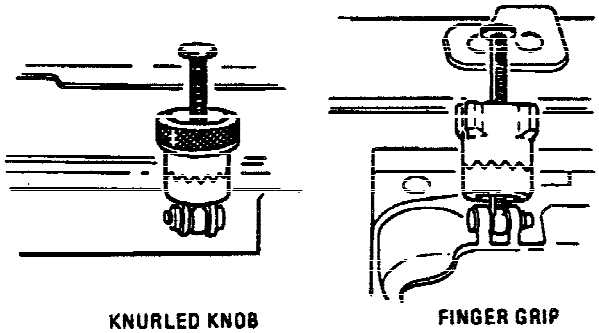
c. Channel 10 programmer matrix which routes channel 4 line sensor output to channel 10 line driver when programmer jumper plug W2 is in the program (P) position.

14-24. Programming. At the present time, no programming is required. All programmer jumper plugs are to be in the stowed position.

14-25. **SPECIAL MAINTENANCE REQUIREMENTS.**

14-26. **FASTENERS.** Refer to applicable paragraph below.

14-27. **LRU Spring Lock Fastener Loosening and Tightening.**



CAUTION

To prevent damage to fasteners, do not use hand tools to loosen or tighten knobs.

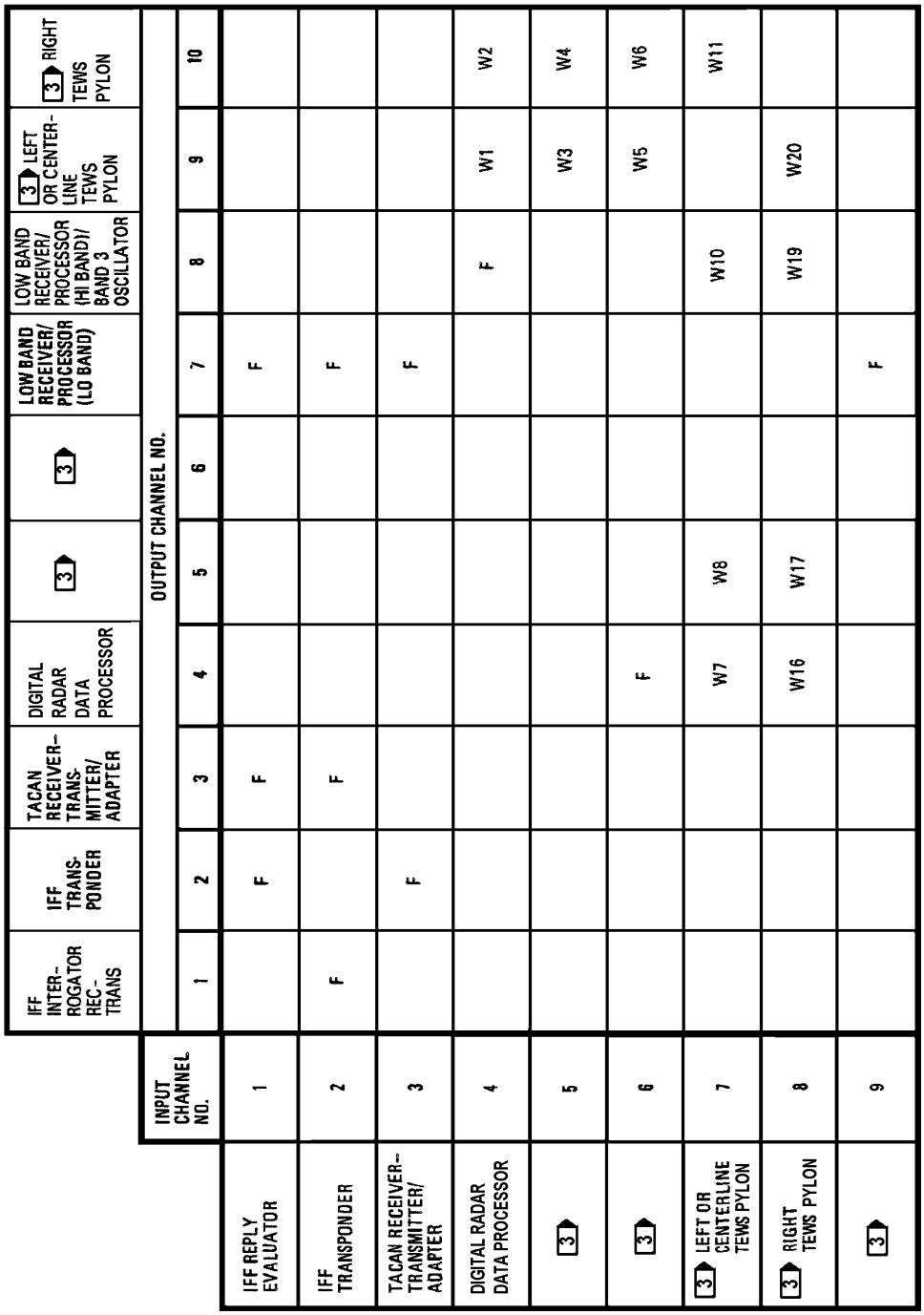
NOTE

Two types of LRU spring lock fasteners are used. One fastener has a knurled knob and the other a knob with four finger grips.

14-28. Loosening.

1. Pull knob out to release serrated collar and turn CCW until knob no longer engages collar when released.
2. Turn knob CCW until collar can be pulled up enough to rotate swivel bolt down to clear mounting foot on LRU.

Table 14-1. Input/Output Distribution Matrix



INPUT CHANNEL NO.		OUTPUT CHANNEL NO.									
		1	2	3	4	5	6	7	8	9	10
		IFF INTER-ROGATOR REC-TRANS	IFF TRANS-PONDER	TACAN RECEIVER-TRANS-MITTER/ ADAPTER	DIGITAL RADAR DATA PROCESSOR	[3]	[3]	LOW BAND RECEIVER/ PROCESSOR (LO BAND)	LOW BAND RECEIVER/ PROCESSOR (HI BAND)/ BAND 3 OSCILLATOR	[3] LEFT OR CENTER-LINE TEWS PYLON	[3] RIGHT TEWS PYLON
IFF REPLY EVALUATOR	1		F	F				F			
IFF TRANSPONDER	2	F		F				F			
TACAN RECEIVER-TRANSMITTER/ ADAPTER	3		F					F			
DIGITAL RADAR DATA PROCESSOR	4								F	W1	W2
[3]	5									W3	W4
[3]	6				F					W5	W6
[3] LEFT OR CENTERLINE TEWS PYLON	7				W7	W8			W10		W11
[3] RIGHT TEWS PYLON	8				W16	W17			W19	W20	
[3]	9							F			

LEGEND

1. WXX-PROGRAMMER JUMPER PLUG NUMBER.
2. F-FIXED DISTRIBUTION.
3. [3] NOT USED.

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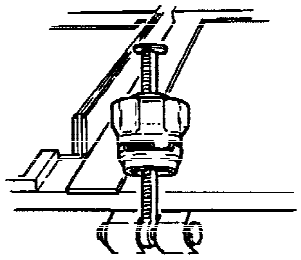
14-29. Tightening.

1. Rotate swivel bolt up until serrated collar engages mounting foot on LRU.
2. Turn knob CW until knob is tight.
3. Gently push LRU in and turn knob until tight.

14-30. LRU Ratchet Fastener Loosening and Tightening.



CAUTION

To prevent damage to fasteners, do not use hand tools to loosen or tighten knobs.

14-31. Loosening.

1. Turn knob CCW until swivel bolt can be rotated to clear mounting foot on LRU.

14-32. Tightening.

1. Rotate swivel bolt up to engage LRU mounting foot.
2. Turn knob CW to tighten knob.
3. Gently push LRU in and turn knob again until tight.

14-33. **CONSUMABLE MATERIALS LIST.**

14-34. **SUPPLIES (CONSUMABLES).** A list of supplies required is provided in Table 14-2.

Table 14-2. Supplies (Consumables)

System/ Nomenclature	Material	Part Number (Mfg. Code)
Blanker (None required)		

14-35. **SUPPORT EQUIPMENT LIST.**

14-36. **TEST EQUIPMENT.** Test equipment required for maintenance of the Blanker is listed in Table 14-3.

Table 14-3. Test Equipment List

System/Equipment Number	Nomenclature	Use and application
AN/PSM-37 AN/PSM-6( ) (Alternate)	Multimeter	Trouble analysis

14-37. **SPECIAL TOOLS.** Special tools required for maintenance of the Blanker is listed in Table 14-4.

Table 14-4. Special Tools List

System/Equipment Number	Nomenclature	Use and application
	Maintenance stand	99-14-11

SECTION XV

COUNTERMEASURES DISPENSER SET AN/ALE-45 (CMD)

15-1. **SYSTEM FUNCTIONAL DESCRIPTION.**

15-2. This section contains maintenance instructions for Countermeasures Dispenser Set AN/ALE-45 (referred to as CMD) which is made up of the equipment listed in Table 15-1. The CMD is part of the tactical electronic warfare system (TEWS).

15-3. The function of the CMD is to dispense and manage chaff, IR flare, and/or other expendable countermeasure payloads. In completing this function, the CMD receives threat information from the AN/ALR-56C (RWR). The CMD determines the best dispense program based on CMD mode, payload management inputs, available payload, threat type, altitude, velocity and aspect angle. Two expendable stores magazines are mounted in each dispenser switch assembly (DSA). Two dispenser switch assemblies are installed on each side of the aircraft.

15-4. **DESCRIPTION.** See Figures 15-1 and 15-2. The CMD, under preprogrammed or RWR control, determines which expendable countermeasures payloads will counter the most immediate threats. Mode selection on the CMD control panel initiates CMD programmer control of the dispense or BIT program. The dispense program can be started either automatically or manually. Commands to the DSA start firing, if ground pins are removed and weight is off aircraft wheels. CMD status is displayed on the TEWS Displays Unit, BIT control panel, and TEWS indicator lights panel.

15-5. **LINE REPLACEABLE UNITS.** CMD line replaceable units (LRU) are identified and listed in Table 15-1.

Table 15-1. Line Replaceable Units

Common Name	S/S/SN	Ref Des	Nomenclature
CMD Control Panel	99-15-11	70Z-J006	CMD Control Panel Assembly
DSA - L Aft	99-15-14	70Z-P002	Dispensing Switch Assembly SA-2281/ALE-45
DSA - L Fwd	99-15-14	70Z-P001	Dispensing Switch Assembly SA-2281/ALE-45
DSA - R Aft	99-15-14	70Z-R004	Dispensing Switch Assembly SA-2281/ALE-45
DSA - R Fwd	99-15-14	70Z-R003	Dispensing Switch Assembly SA-2281/ALE-45
DSA Safety Switch - L	99-15-13	70S-P012	Switch
DSA Safety Switch - R	99-15-13	70S-R013	Switch
CMD Programmer	99-15-10	70Z-F005	Electronic Command Signal Programmer C-10704/ALE-45
TEWS Indicator Lights Panel	99-15-12	52Z-J376	Indicator Light Assembly

15-6. **COMPONENT DESCRIPTION.** The paragraphs below describe the CMD units. Each unit is hard mounted.

15-7. **CMD Control Panel (99-15-11).** The CMD control panel allows control of stores management operational mode and emergency modes of the CMD operation.

15-8. **DSA (99-15-14).** The DSA's are identical and interchangeable. The DSA receives management, BIT, and firing commands from the programmer. The DSA's fire the expandable stores in either of the two expendable stores magazines. The firing circuit status and stores remaining are data linked back to the CMD programmer.

15-9. **DSA Safety Switches (99-15-13).** The DSA safety switches make sure DSA firing voltage is interrupted during ground servicing.

15-10. **CMD Programmer (99-15-10).** The programmer maintains communication with the RWR exchanging threat and display data. A microprocessor within the CMD programmer maintains control with inputs from cockpit controls and CMD control panel. The CMD programmer controls the L Aft, L FWD, R Aft, and R FWD DSA's.

15-11. **TEWS Indicating Lights Panel (99-15-12).** Indicates that chaff or flares are being dispensed or when predetermined expendable stores minimum has been reached. Also indicates when dispense action is required.

15-12. **RELATED COMPONENT DESCRIPTION.**

15-13. **TEWS Display Unit.** The TEWS display unit, a component of the RWR, is used to display program number and expendable stores inventory.

15-14. **PRINCIPLES OF OPERATION.** See Figure 15-2. The CMD principles of operation include a description of operating controls and indicators, and operation of the system functions as below:

a. Power and Control

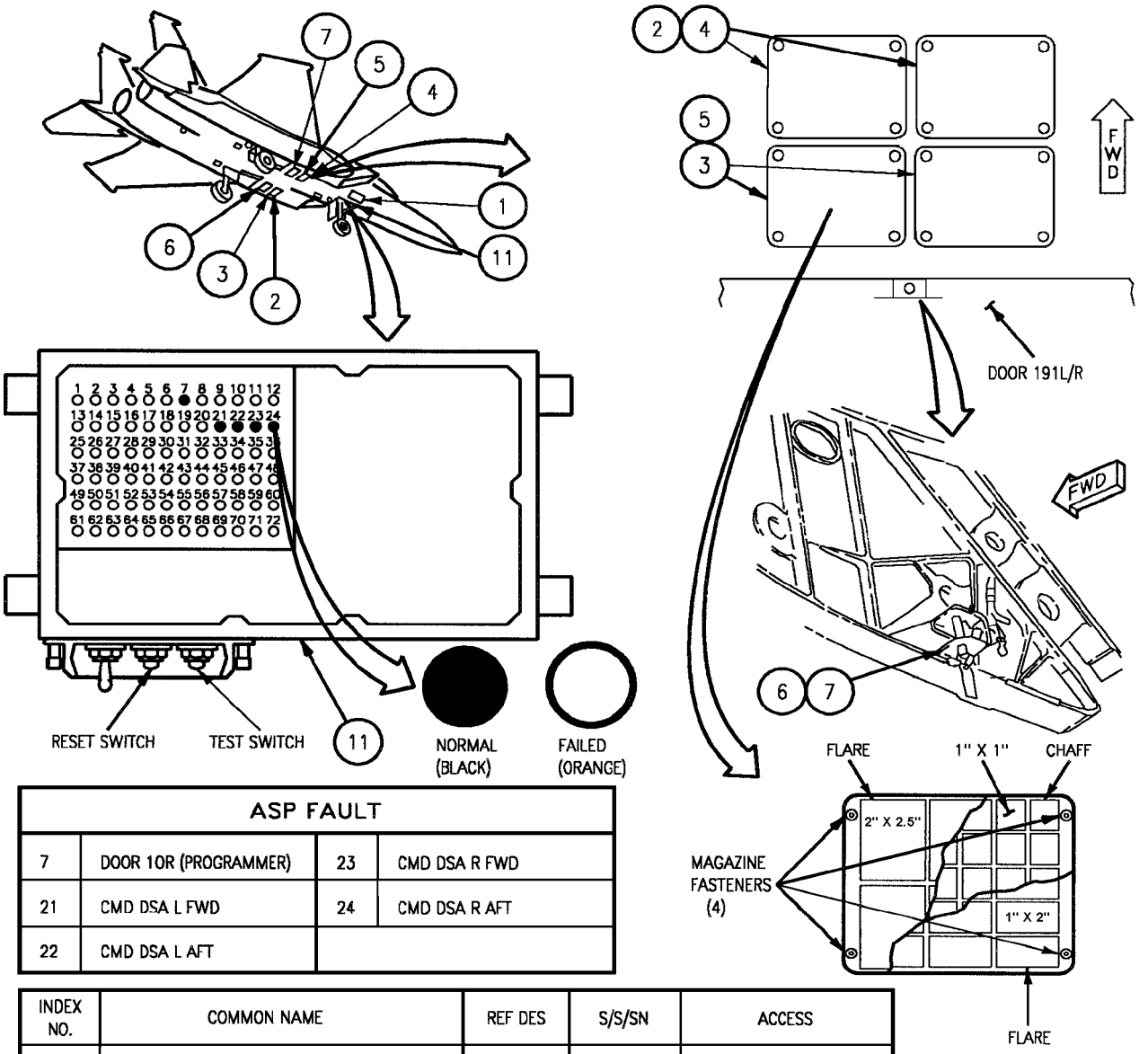
b. Logic and Firing

c. Bit

15-15. **Controls and Indicators.** All controls and indicators used in CMD operation are shown in Figure 15-1 and described in Table 15-2.

Table 15-2. Controls and Indicators

Control/Indicator	Position/Condition	Function/Indication
CMD Control Panel		
Mode Switch	OFF	a. Applies CMD off to CMD programmer. b. With weight-off-wheels, FLARE jettison switch in Jett, all flares will be dispensed.
	STBY	Full initiated BIT possible only in this mode. Power up and continuous BIT possible in all modes; no dispensing of payload cartridges.
	MAN ONLY	a. Dispenser switch actuated (down) will start manual 2 dispense program per EEPROM memory as selected by the DISP SEL switch. The EEPROM program will be determined by the CMD MSS and/or the PFM load. b. Actuation of the autopilot/ steering disengage switch twice, with autopilot engaged, will start a manual 1 program per EEPROM memory, which is controlled by the CMD MSS and/or the PFM load.



ASP FAULT			
7	DOOR 10R (PROGRAMMER)	23	CMD DSA R FWD
21	CMD DSA L FWD	24	CMD DSA R AFT
22	CMD DSA L AFT		

INDEX NO.	COMMON NAME	REF DES	S/S/SN	ACCESS
1	CMD PROGRAMMER	70Z-F005	99-15-10	DOOR 10R
2	DSA - L FWD	70Z-P001	99-15-14	DOOR 191L
3	DSA - L AFT	70Z-P002	99-15-14	DOOR 191L
4	DSA - R FWD	70Z-R003	99-15-14	DOOR 191R
5	DSA - R AFT	70Z-R004	99-15-14	DOOR 191R
6	DSA SAFETY SWITCH - L	70S-P012	99-15-13	DOOR 52L
7	DSA SAFETY SWITCH - R	70S-R013	99-15-13	DOOR 52R
8	CMD CONTROL PANEL (INTERCHANGEABLE)	70Z-J006	99-15-11	COCKPIT
9	TEWS DISPLAY UNIT	65Z-J009	99-11-13	COCKPIT
10	BIT CONTROL PANEL	66Z-H002	31-50-11	COCKPIT
11	AVIONICS STATUS PANEL	66Z-G001	31-50-10	NLG WHEELWELL
12	ESSENTIAL BUS CIRCUIT BREAKER PANEL	52Z-C007	24-50-12	DOOR 6L
13	LEFT THROTTLE GRIP DISPENSER SWITCH	52Z-H030	76-10-26	COCKPIT
14	TEWS CONTROL PANEL	65Z-J010	99-11-14	COCKPIT
15	TEWS INDICATOR LIGHTS PANEL	52Z-J376	99-15-12	COCKPIT
16	AUTOPILOT/STEERING DISENGAGE SWITCH	93Z-J005	22-10-23	COCKPIT
1 ▶ 17	AUTOPILOT/STEERING DISENGAGE SWITCH	93Z-L002	22-10-23	REAR COCKPIT
18	MULTIPURPOSE COLOR DISPLAY	61Z-H003	94-10-27	COCKPIT

LEGEND

1 ▶ F-15D

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Figure 15-1. Countermeasures Dispenser Set AN/ALE-45 (Sheet 1 of 4)

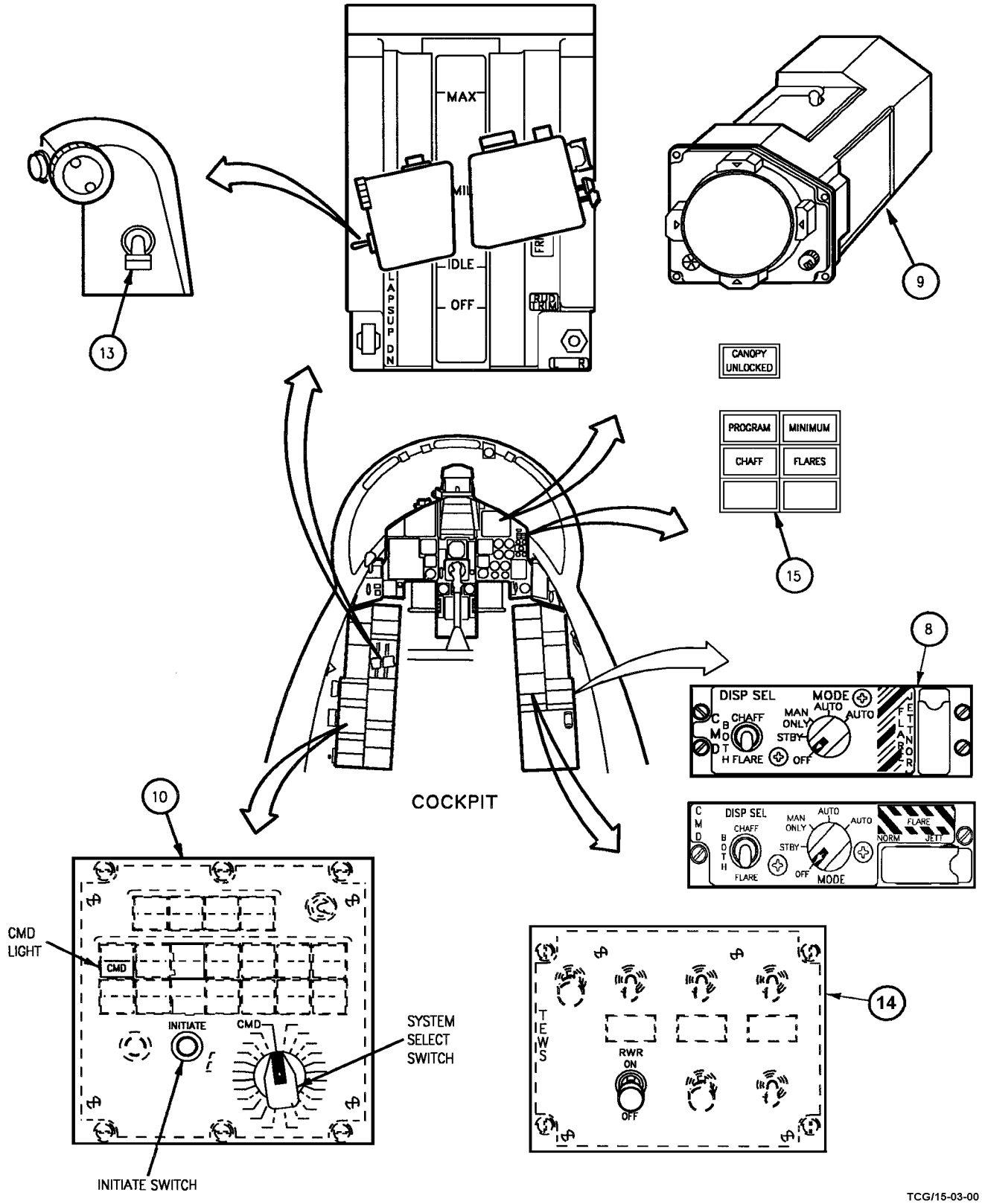


Figure 15-1. Countermeasures Dispenser Set AN/ALE-45 (Sheet 2)

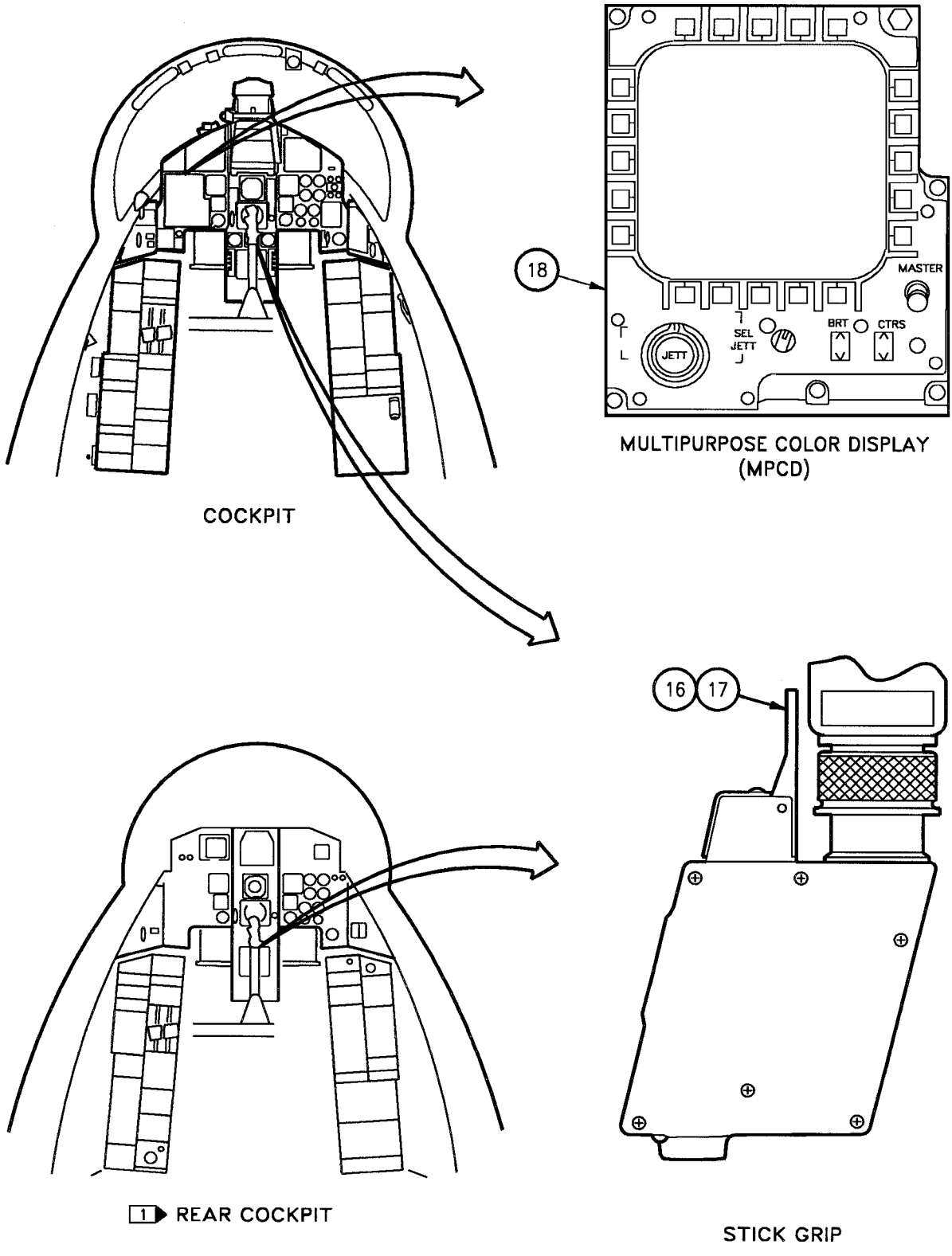
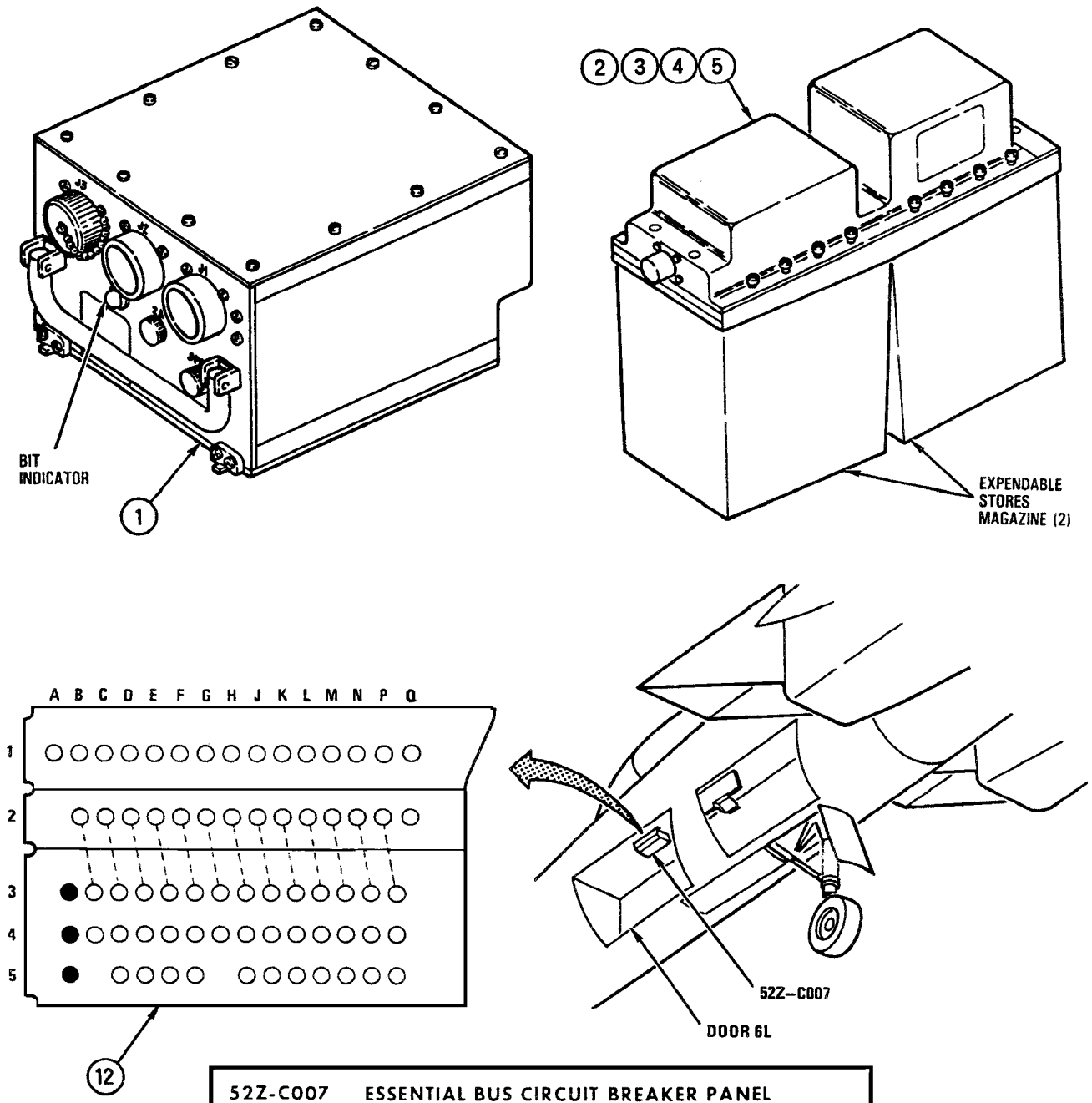


Figure 15-1. Countermeasures Dispenser Set AN/ALE-45 (Sheet 3)



52Z-C007 ESSENTIAL BUS CIRCUIT BREAKER PANEL			
REF DES	ZONE	NOMENCLATURE	BUS
70CBC007 70CBC009 70CBC011	A3 A4 A5	CMD DSA FWD CMD DSA AFT CMD PRGMR	28VDC 28VDC 28VDC

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Figure 15-1. Countermeasures Dispenser Set AN/ALE-45 (Sheet 4)

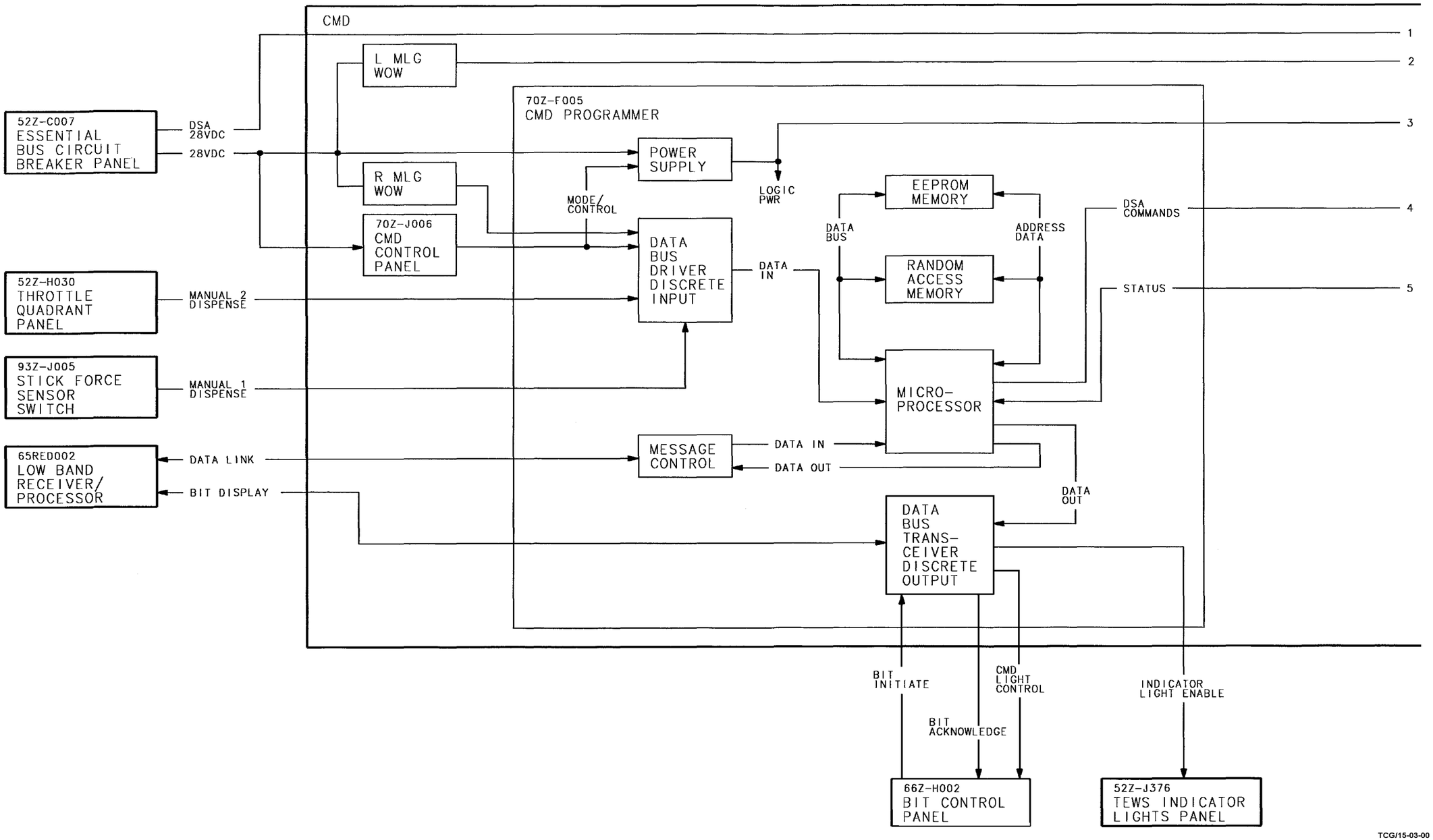

Figure 15-2. CMD Functional Block Diagram (Sheet 1 of 2)

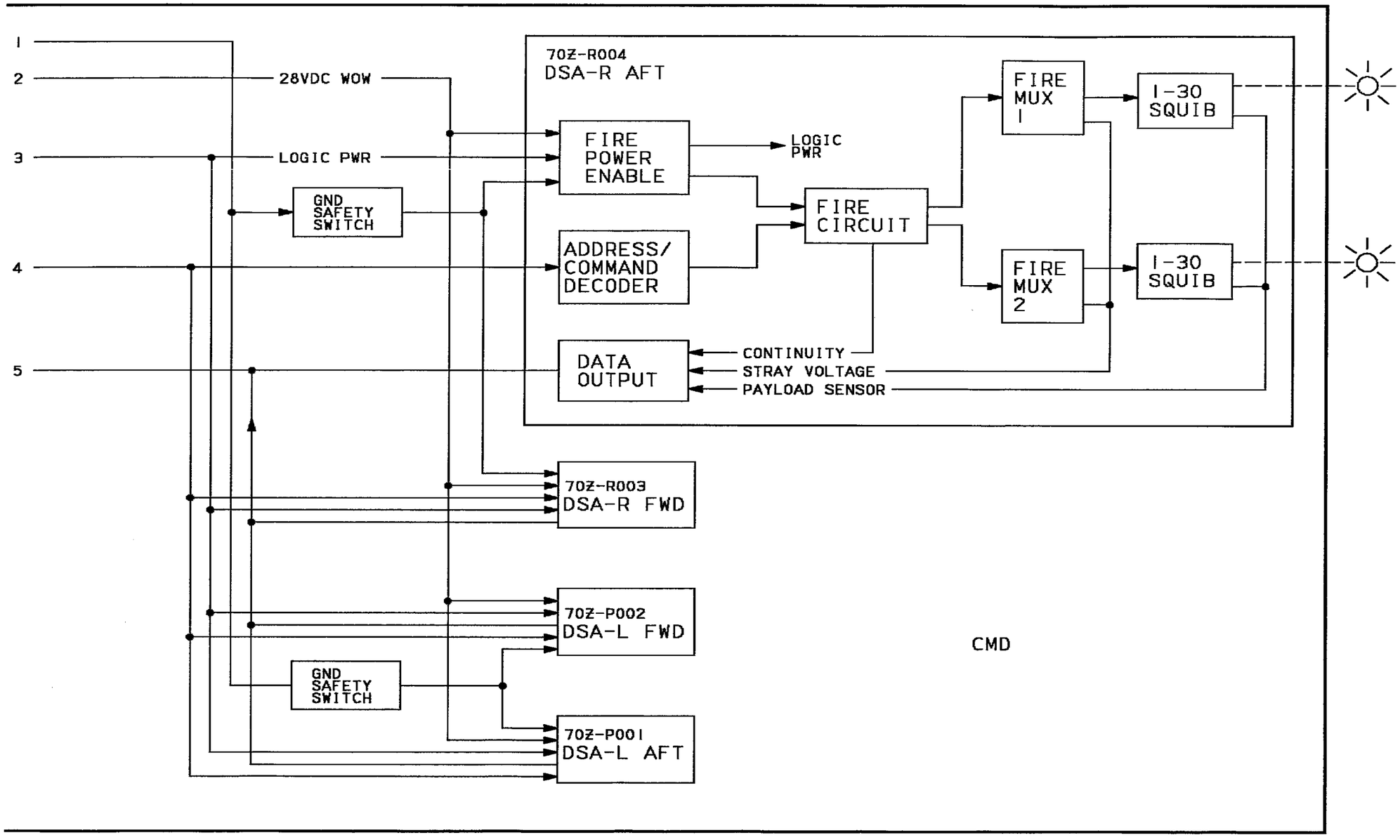

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Figure 15-2. CMD Functional Block Diagram (Sheet 2)

Table 15-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
		c. Actuation of the autopilot/ steering disengage switch once while autopilot is disengaged, will start a manual 1 program per EEPROM memory, which is controlled by the CMD MSS and/or the PFM load.
	SEMI AUTO	a. With PROGRAM light on, dispenser switch actuation (down) starts RWR dispense program. A second actuation will replace RWR dispense with a manual 2 dispense program.
		b. With no RWR threats identified, and dispenser switch actuated (down); chaff, flare or both will be dispensed as selected by the DISP SEL switch per manual 2 dispense program.
	AUTO	a. With RWR dispense program in process, dispenser switch actuation (down) will start a manual 2 dispense program.
		b. With no RWR threats identified and dispenser switch actuated (down), chaff, flare or both will be dispensed as selected by the DISP SEL switch per manual 2 dispense program.
DISP SEL Switch	CHAFF (OPT 1)	a. With mode switch in MAN ONLY, activating the manual 1 or manual 2 dispense program will dispense chaff and/or flare per the PFM load or the manually selected CMD MSS program on the MPCD.
		b. Chaff will be dispensed during a manual 2 dispense program (dispenser switch actuated) with mode switch in SEMI AUTO or AUTO and no RWR threats identified.
	FLARE (OPT 3)	a. With mode switch in MAN ONLY, activating manual 1 or manual 2 dispense program will dispense chaff and/or flare per the PFM load or the manually selected CMD MSS program on the MPCD.
		b. Flares will be dispensed during a manual 2 dispense program (dispenser switch actuated) with mode switch in SEMI AUTO or AUTO and no threats identified.

Table 15-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
	BOTH (OPT 2)	a. With mode switch in MAN ONLY, activating the manual 1 or manual 2 dispense program will dispense chaff and/or flare per the PFM load or the manually selected CMD MSS program on the MPCD. b. Chaff and flares will be dispensed during a manual 2 dispense program (dispenser switch actuated) with mode switch in SEMI AUTO or AUTO and no RWR threats identified.
FLARE JETT switch	NORM	Emergency flare jettison inhibited.
	JETT	With weight-off-wheels, all flares will be dispensed. Other dispensables may be dispensed.
TEWS Indicator Lights Panel		
MINIMUM Light	On (steady)	When expendable countermeasure payloads reach predetermined software level.
	OFF	When expendable countermeasure payload reaches zero.
	On (flashing)	During time of initiated BIT.
PROGRAM Light	On (steady)	In SEMI AUTO mode, indicates RWR has provided a stored dispense program. Pilot action required.
	On (flashing)	During time of initiated BIT.
	OFF	a. SEMI AUTO mode is not selected. b. IN SEMI AUTO mode; but, no dispense program provided by RWR
CHAFF Light	On (steady)	Chaff expendable stores magazine installed but empty.
	On (flashing - rate programmable)	a. When dispensing chaff. b. During time of initiated BIT.
FLARE Light	On (steady)	Flare expendable stores magazine installed but empty.
	On (flashing - rate programmable)	a. When dispensing flares. b. During time of initiated BIT.

Table 15-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
1 Throttle Quadrant Panel		
Dispenser Switch	Down (spring loaded to center)	a. In AUTO mode with RWR dispense program in process, a manual 2 dispense program will be started. b. IN AUTO or SEMI AUTO mode, with no RWR threats identified; chaff, flare or both chaff and flares will be dispensed as selected by the DISP SEL switch per manual 2 dispense program. c. In SEMI AUTO mode with PROGRAM light on, RWR dispense program will be started. A second actuation will replace RWR dispense program with a manual 2 dispense program. d. In MAN ONLY mode.
Throttles	Advanced to afterburner	Increases the number of flares dispensed.
1 Stick Force Sensor		
Autopilot/Steering disengage switch	MAN ONLY	a. Actuation of the autopilot/ steering disengage switch twice, with autopilot engaged, will start a manual 1 program per EEPROM memory, which is controlled by the PFM load or the manually selected CMD MSS on the MPCD. b. Actuation of the autopilot/ steering disengage switch once while autopilot is disengaged, will start a manual 1 program per EEPROM memory.
1 BIT Control Panel		
System select switch	CMD	In CMD position, selects and tells CMD when manual BIT is to be done.
INITIATE switch	Press and release	Full initiated BIT only in STBY. In MAN ONLY, SEMI AUTO, and AUTO, only initiated inventory BIT possible.
CMD light	On (steady)	a. When CMD is off. b. When CMD is on and a CMD failure occurs.
	On (flashing)	a. Flashes for approximately 10 seconds during time duration of initiated BIT cycle and then goes off.

Table 15-2. Controls and Indicators (CONT)

Control/Indicator	Position/Condition	Function/Indication
	Not on	When CMD is on and operating normally.
[1] **Multipurpose Color Display**		
Menu		
S01	Press and release	Displays Armament
S03	Press and release	Displays SIT
S09	Press and release	Displays AUTO RANGE.
S11	Press and release	Displays DECLUTTER
S12	Press and release	Displays LINES.
S15	Press and release	Displays TIME/DATE.
ARMAMENT display selected from MENU		
	Press and release	Displays total Chaff and Flare quantities.
SIT display selected from MENU		
	Press and release	Displays total Chaff and Flare quantities.
[1] Related to but not part of Countermeasures Dispenser system.		

15-16. **Display Presentations.** See Figure 15-3. During initiated BIT, a display appears on the TEWS display unit. The upper numbers (three sets of two), reading left to right, indicate flight program, preflight message, and patch number respectively. The lower numbers which follow 1 through 6 indicate the inventory of expendables which remain in the CMD.

15-17. During flight or ground maintenance, with weight-off-wheels switch enabled and RWR in the operate mode, the total chaff and flare quantities will be displayed on the MPCD in two different displays. The tactical situation and the PACS air to air display. On the tactical situational display, the total quantities are displayed in the lower right corner of the display (see Figure 15-3, detail A). The total quantities will be displayed as two lines of data. The first line displays a C followed by the total number of RR-170 and RR-180 chaff bundles. The second line displays an F followed by the total number of MJU-7 and MJU-10 flares. Each line will be displayed in a color that corresponds to the current total quantities of each line. Green indicates that the total quantities of stores is above the minimum amount. Amber indicates that the total quantities of stores are at or below the minimum quantity but above zero. Magenta (red) indicates the total quantity of stores is zero.

15-18. The third line of data is used to indicate the type of programmed dispense sequence used to release the chaff or flares. MSS indicates that a manually entered dispense program is being used by the CMD. PFM indicates that the dispense program being used originated in the PFM program.

15-19. On the PACS air to air display, the CMD stores total quantity is displayed in the upper right corner of the display (see Figure 15-3, detail C). The chaff and flare inventories are displayed in two lines of data. The first line displays CHF followed by the total quantity of RR-170 and RR-180 chaff bundles. The second line displays FLR followed by the total quantity of MJU-7 and MJU-10 flares. Each line is displayed in a color

that corresponds to the current total quantities of each line. Green indicates that the quantity of stores is above the minimum amount. Amber indicates that the total quantities of stores are at or below the minimum quantity but above zero. Magenta indicates the total quantity of stores is zero.

15-20. The third line of data is used to indicate the type of programmed dispense sequence that is currently being used by the CMD to dispense chaff or flares. MSS indicates that a manually entered dispense program is being used by the CMD. PFM indicates that the dispense program being used originated in the PFM program.

15-21. **Power and Control.** See Figure 15-4. Primary power of 28VDC is routed to the reset circuit in the CMD programmer, the CMD control panel, both DSA safety switches, each DSA and several relays. The reset circuit supplies 28VDC power to the power supply and 28VDC logic power to all DSA as long as 28VDC is present from the CMD control panel. Inhibit is not applied to the power supply at this time. The power supply produces 5VDC and -5VDC logic power to operate the CMD programmer circuits.

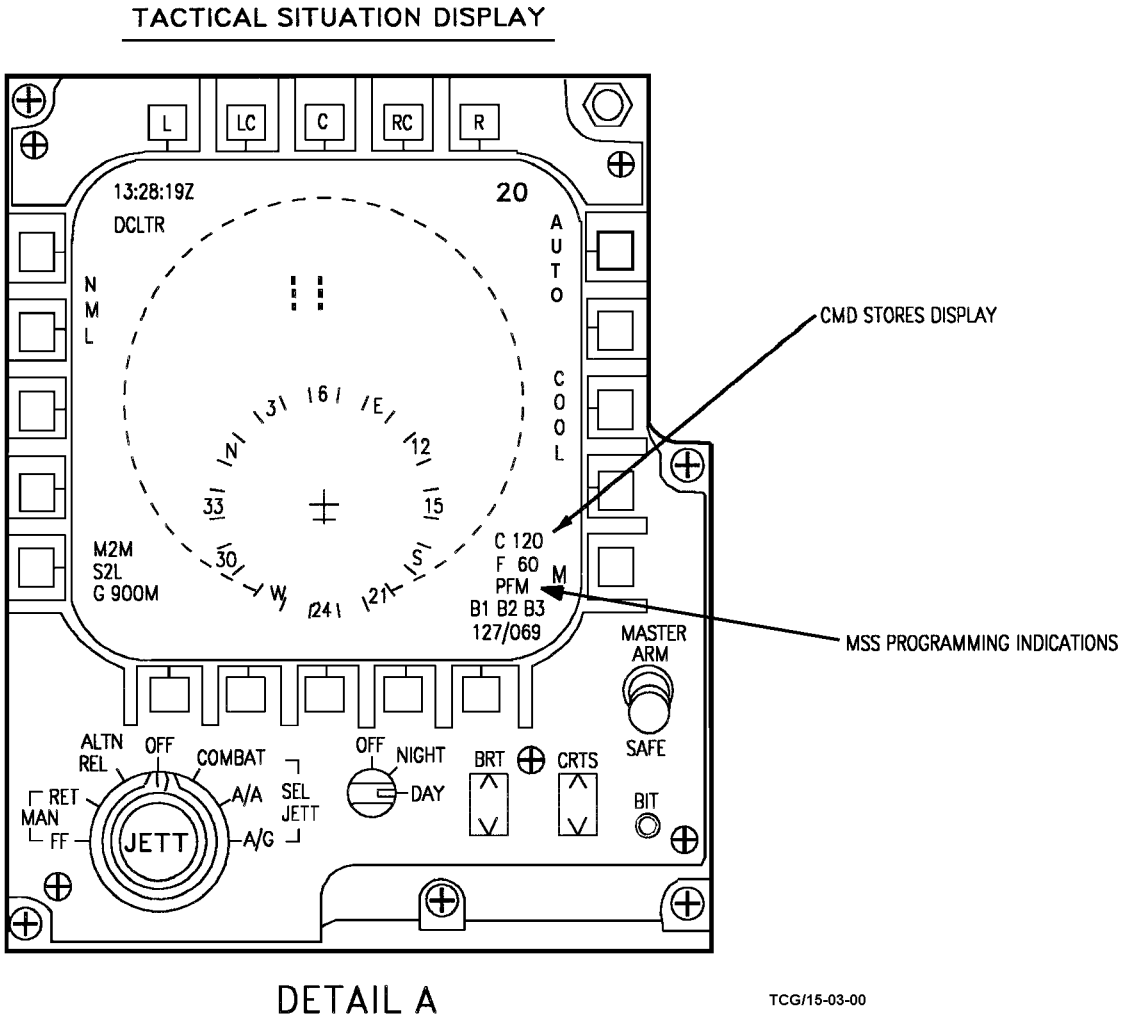

Figure 15-3. Countermeasures Dispenser Set Displays (Sheet 1 of 3)

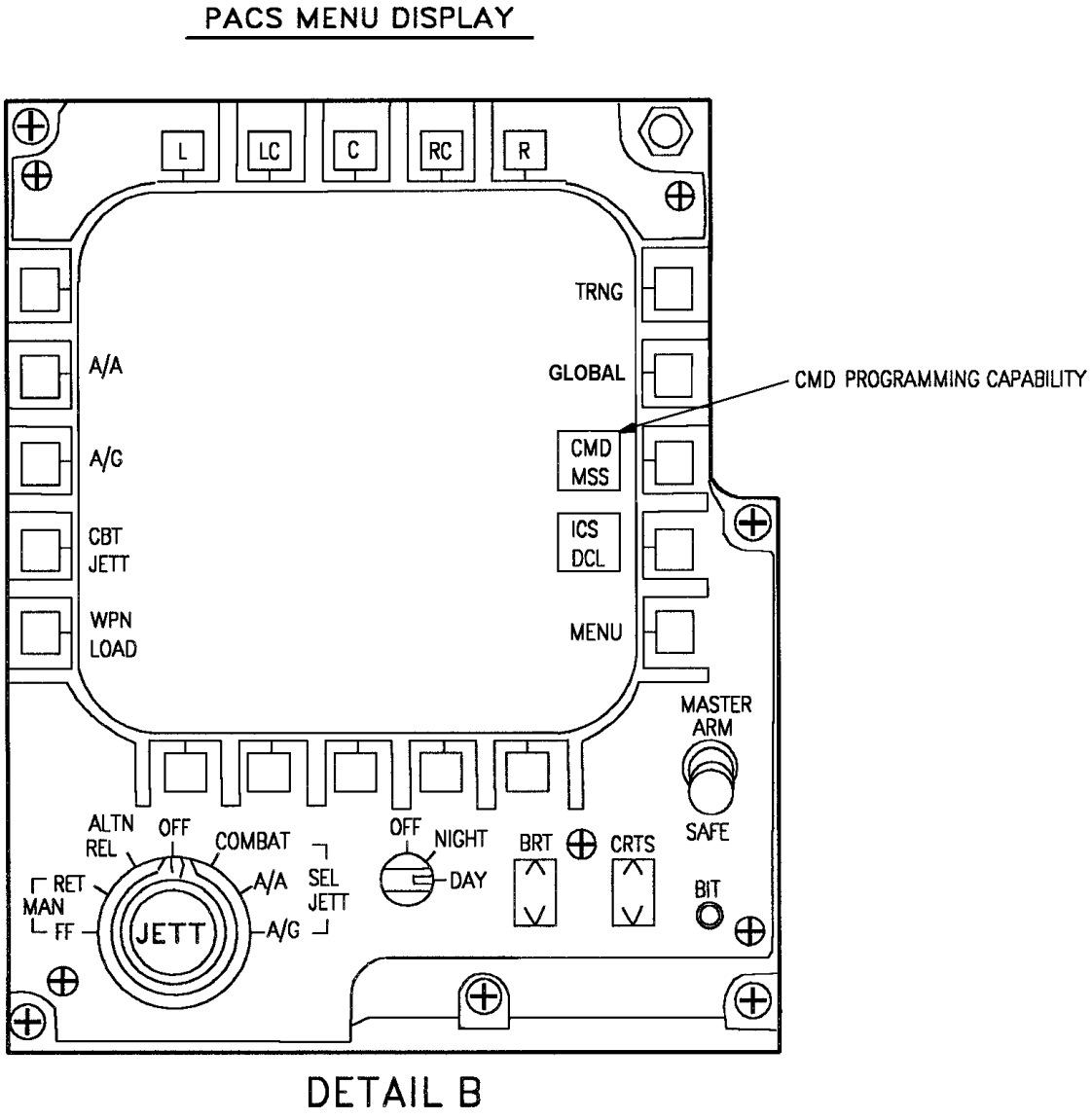

Figure 15-3. Countermeasures Dispenser Set Displays (Sheet 2)

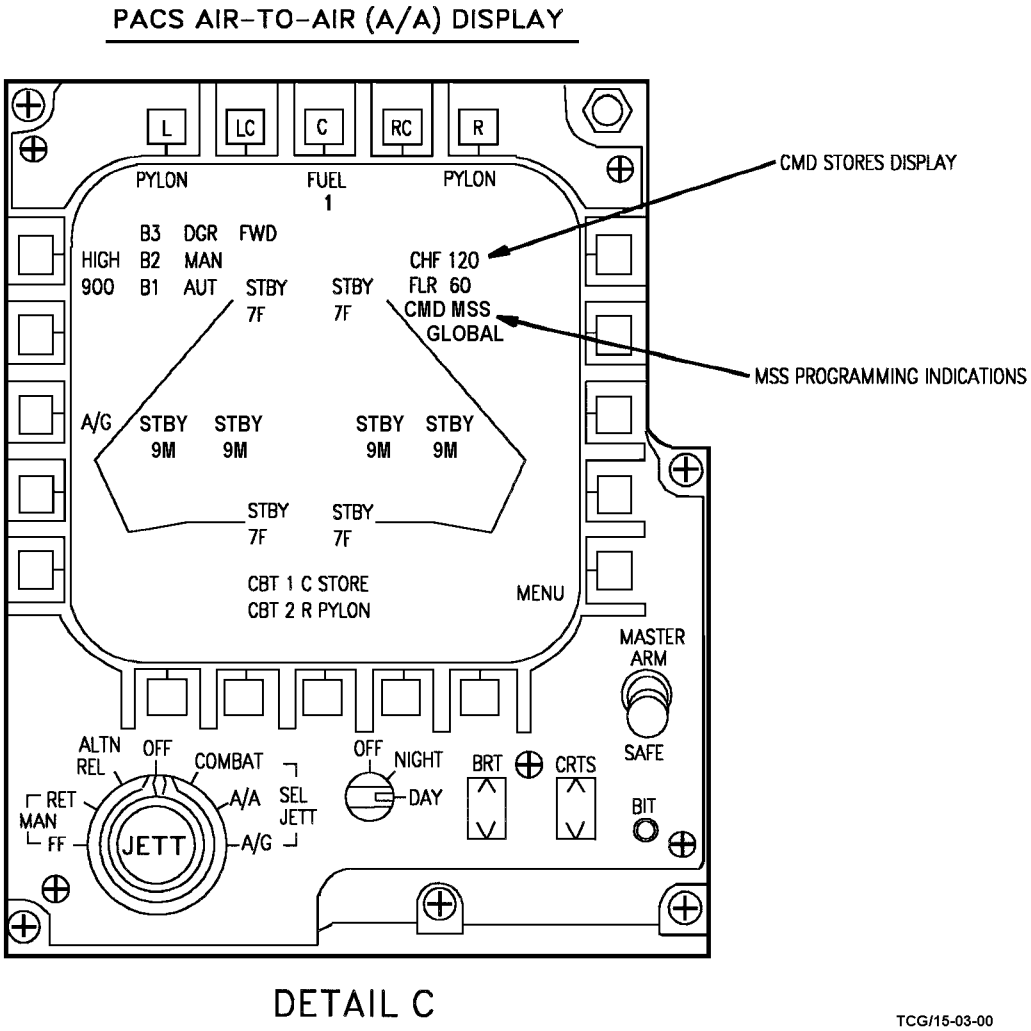

Figure 15-3. Countermeasures Dispenser Set Displays (Sheet 3)

15-22. The 28VDC to the CMD control panel is used for mode switching. The mode switching signals are applied to the data bus driver discrete input, reset and interrupt control in the CMD programmer. In MAN ONLY, SEMI AUTO, or AUTO mode, a ground by the MODE switch is applied to the No. 4 Miscellaneous Relay Panel autopilot disengage relay 93K-R034. Relay 93K-R034 will be deenergized when autopilot/ steering disengage switch is actuated while the autopilot is disengaged. Relay 93K-R034 is also deenergized when autopilot/steering disengage switch is actuated twice and the autopilot is engaged while airborne.

15-23. On F-15C, when deenergized, 93K-R034. applies the ground to K2 in Avionics Miscellaneous Modular Relay Panel No. 9. Relay K2 is deenergized when the autopilot/disengage switch is actuated. A ground energizes the man prog 1 dispense relay K1. When energized, a ground is applied to the data bus driver discrete input of the CMD programmer as a manual prog 1 dispense command.

15-24. On F-15D, when deenergized, 94K-R034 applies a ground to 55K-Y002 in Avionics Relay Panel No. 7. Relay 55K-Y002 is deenergized when the autopilot/steering disengage switch is actuated, the ground energizes the man prog 1 dispense relay 55K-Y001. When 55K-Y001 is energized, a ground is applied to the CMD programmer as a manual prog 1 dispense command.

15-25. On F-15C 79-0015 THRU 81-0002, F-15D 79-0004 THRU 81-0003 BEFORE TO SR1F-15-1019 when weight is off the main landing gear, primary 28VDC is applied through the energized contacts of the R MLG WOW Relay No. 5 41K-M127. On F-15C 79-0015 THRU 81-0002, F-15D 79-0004 THRU 81-0003 AFTER TO SR1F-15-1019; F-15C 90-0263 AND UP, F-15D 90-0272 AND UP when weight is off the main landing gear, primary 28VDC is applied through the energized contacts of the R MLG WOW Relay No. 5 41K-K127 in the no. 14 Miscellaneous Relay Panel. The 28VDC is applied to the data bus driver input in the CMD programmer. This input, and others from equipment outside the CMD programmer are buffered, converted and transferred to the CPU microprocessor. The 16-bit address controls the timing of data transfer while the 8-BIT DATA BUS contains the information to be loaded into the CPU microprocessor.

15-26. When weight is off the main landing gear, primary 28VDC is applied through the energized contacts of the L MLG WOW Relay No. 1 41K-L027. The 28VDC is applied to the EMI filters in all DSA's. Removal of the safety pin from the DSA safety switch-L allows 28VDC to be applied to DSA-L FWD and DSA-L Aft. Removal of the safety pin from DSA safety switch-R allows 28VDC to be applied to DSA-R FWD and DSA-R Aft.

15-27. The 28VDC logic pwr, 28 VDC fire and 28VDC WOW voltages are applied to the EMI filter. The 28VDC fire and WOW voltages are filtered and used to power the DSA circuits. The 28VDC logic pwr is applied to the +5 and +10VDC reg if 28VDC WOW exists. The output, +5 and +10VDC, is made available for logic power within the DSA. The PWR RESET signal is used to initialize the logic within the DSA.

15-28. **Logic and Firing.** See Figure 15-5. Major circuits are CMD programmer, DSA, and TEWS indicator lights. The CMD programmer is made up of RWR/CMD interface, EEPROM and random access memory, central processing unit (CPU) and output circuits. The manchester receiver/decoder receives inputs from the low band receiver/processor when bit data is not present. The inputs are threat data, request for stores, program identification, aircraft parameters or rebound words. Threat data will include altitude, azimuth, velocity and threat category. Request for stores is made up of the inventory of RR-170 and RR-180 chaff, MJU-7 and MJU-10 flare and any other dispensables. Program identification includes operational flight program (OFP), preflight message (PFM), and Patch No. Aircraft parameters are made up of altitude and velocity. The rebound word is used by the RWR to test the RWR/CMD data link.

15-29. The CPU is the controlling element of the CMD programmer. The CPU microprocessor controls the 16-BIT ADDRESS BUS and 8-BIT DATA BUS. The 16-BIT ADDRESS BUS and 8-BIT DATA BUS interfaces input/output and control functions. The clock logic circuit uses inputs of 1 MHz clock, system clock and memory ready to produce data bus ENABLE. The CPU microprocessor uses reset and power valid to start CPU microprocessor operation. Read/write, bus available gate valid, and memory address are used to control the CPU address bus driver and enable. In addition to the CPU microprocessor inputs, the CPU interrupt control inhibits the CPU ENABLE outputs when a different CMD programmer input exists. The CPU microprocessor analyzes the data stored in

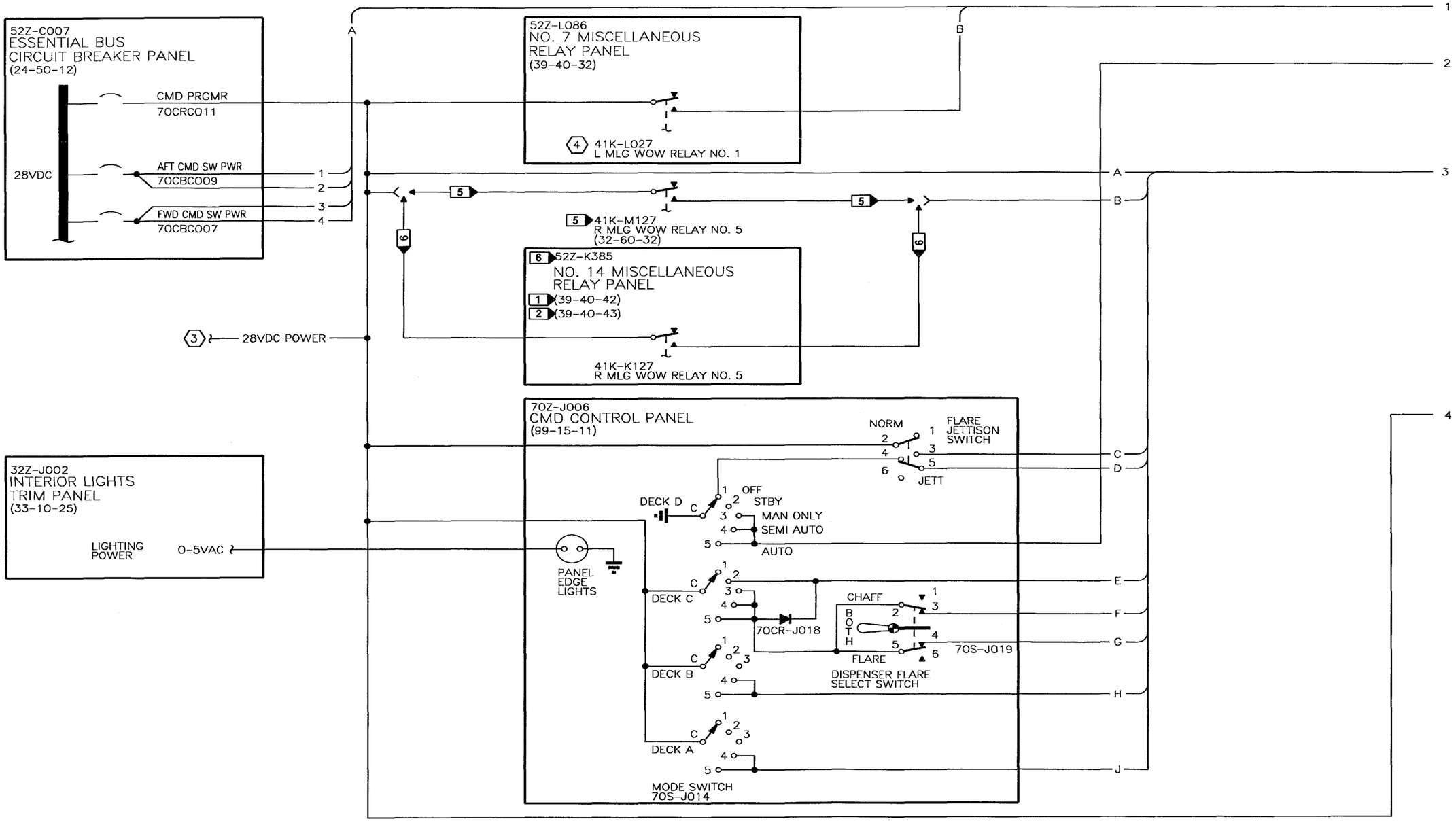

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Figure 15-4. CMD Power and Control Simplified Schematic (Sheet 1 of 4)

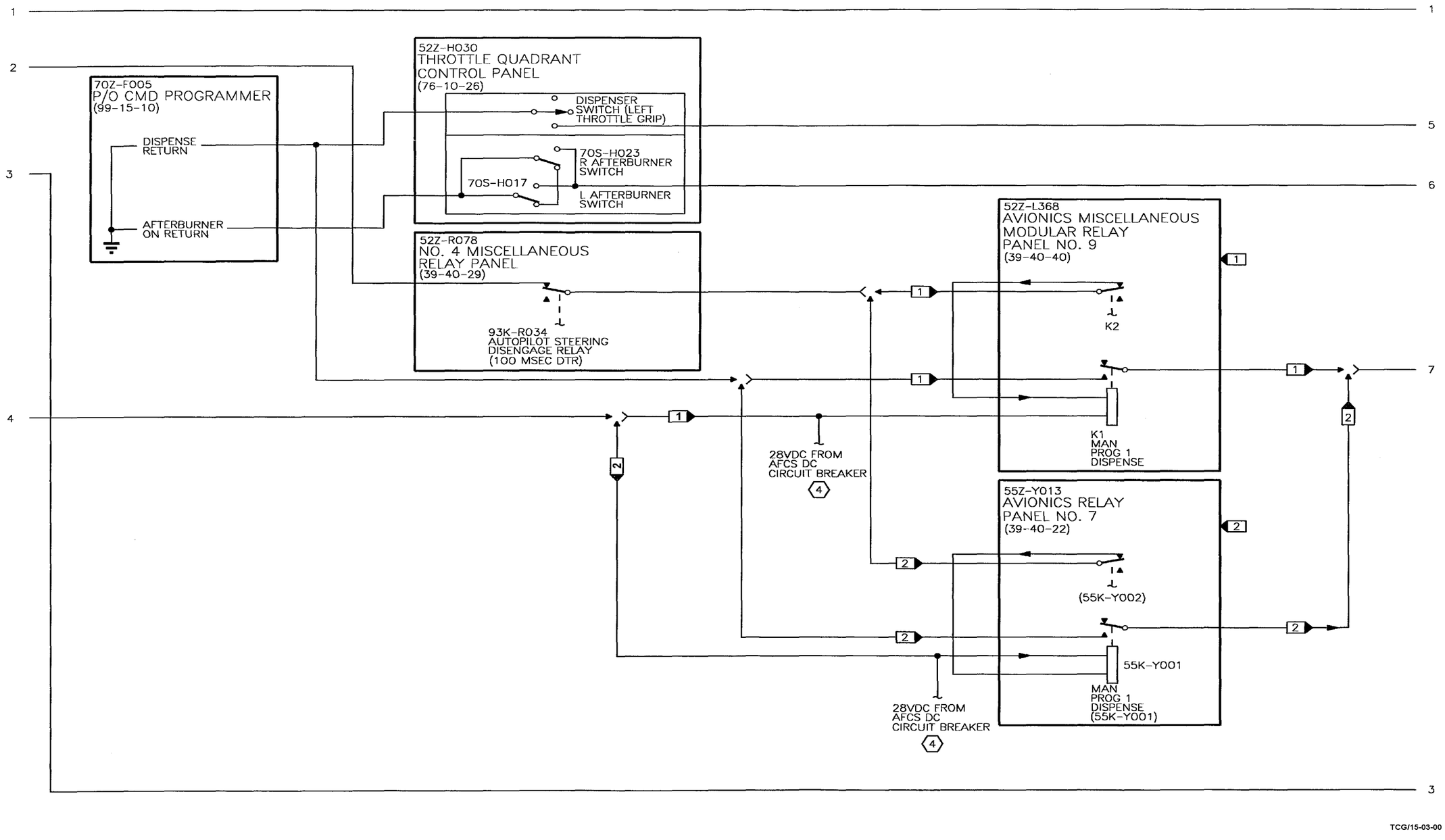

Figure 15-4. CMD Power and Control Simplified Schematic (Sheet 2)

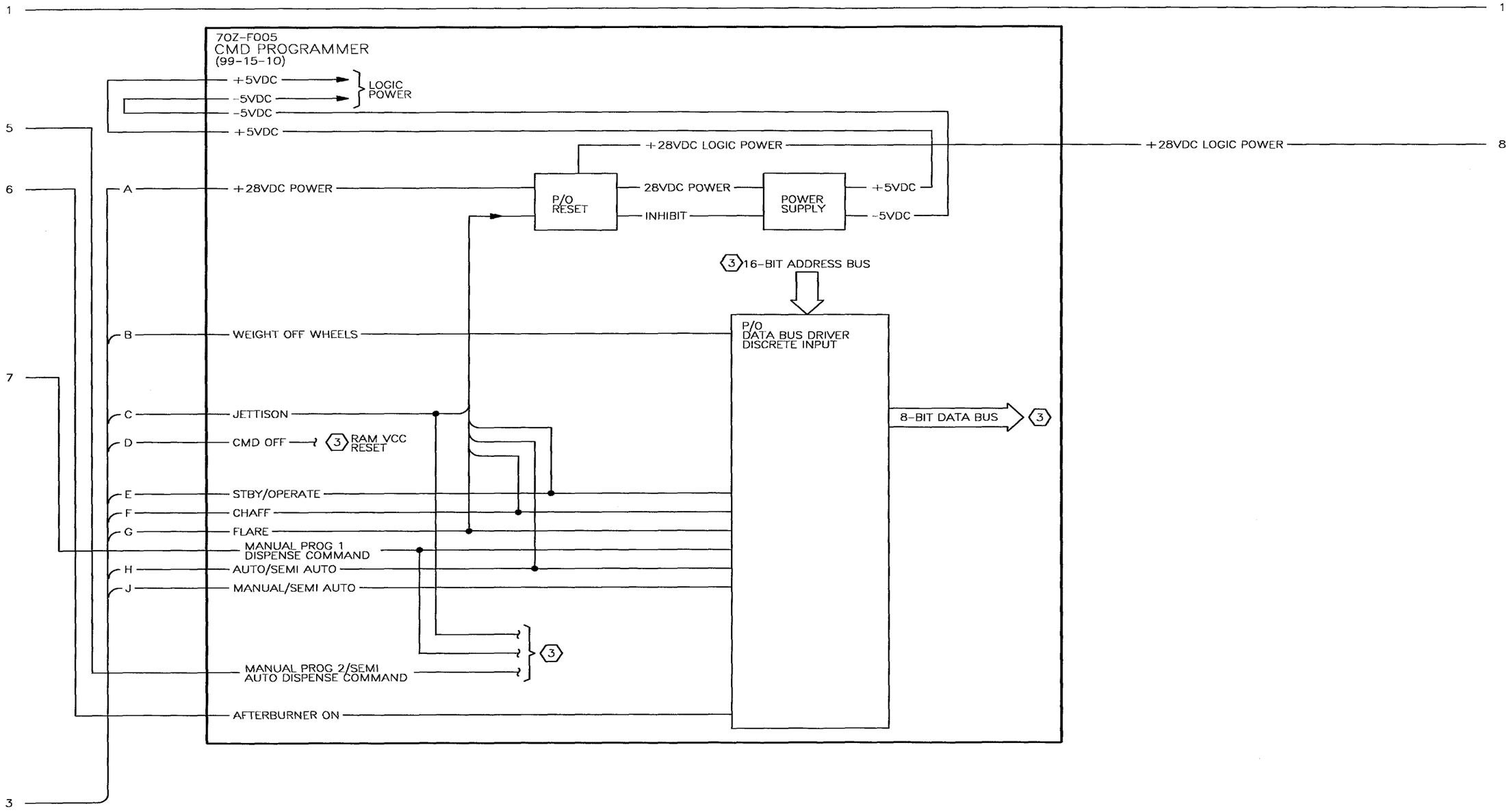

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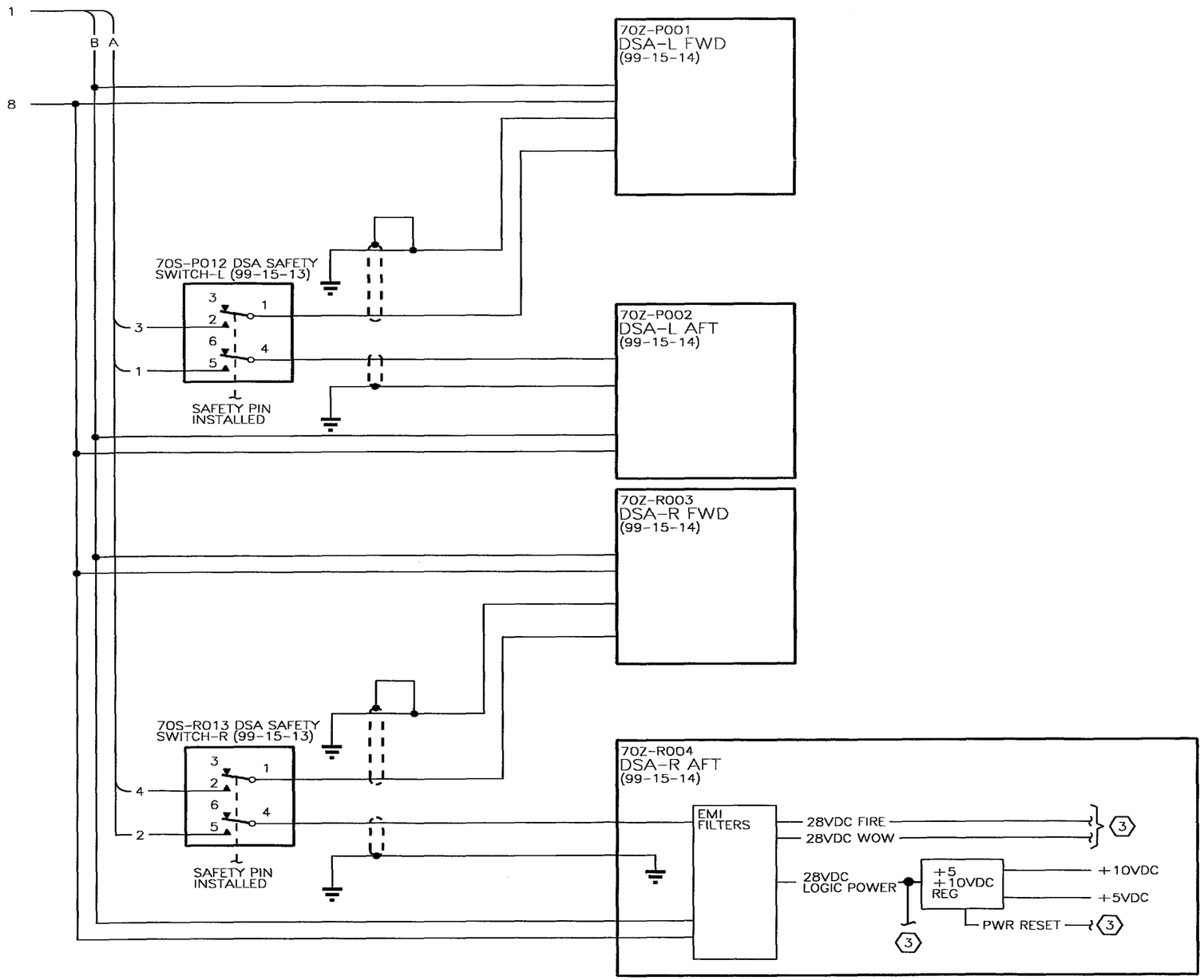
Figure 15-4. CMD Power and Control Simplified Schematic (Sheet 3)



LEGEND

1. F-15C.
2. F-15D.
3. SEE CMD LOGIC AND FIRING SIMPLIFIED SCHEMATIC.
4. SEE AUTO FLIGHT SYSTEM. REFER TO TO SR1F-15C-2-22GS-00-1.
5. **F-15C 79-0015 THRU 81-0002, F-15D 79-0004 THRU 81-0003 BEFORE TO SR1F-15-1019.**
6. **F-15C 79-0015 THRU 81-0002, F-15D 79-0004 THRU 81-0003 AFTER TO SR1F-15-1019; F-15C 90-0263 AND UP, F-15D 90-0272 AND UP.**

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Figure 15-4. CMD Power and Control Simplified Schematic (Sheet 4)

program and data memory using available RWR data and creates firing pattern commands to be sent to the DSA-R Aft, DSA-R FWD, DSA-L Aft and DSA-L FWD. The firing pattern contains elements of timing, DSA status and payload information. Timing information is used to determine time between dispense and completion of dispense action. Status and payload information determine the amount of dispensables available to make the firing pattern.

15-30. The operational flight program(OFP) and PFM, which contains BIT, make up the program memory. The control programs are accessed using address bus driver and data bus transceiver program memory. The EEPROM memory is programmable and defines the functional operation of the CMD. The operational flight program contains information relative to fixed aircraft parameters (altitude and velocity) and threat parameters. The PFM is made up of dispensing parameters. The CPU microprocessor takes the variable information in the random access memory and sees if a match exists within the OFP. If a match is found, specific dispensing parameters are indicated and used to make the firing pattern.

15-31. The data memory is made up of 24 random access memory devices, arranged in twelve pairs. Each pair stores 256 8-bit data words. The data memory is used for variable real-time data. Inventory requests, threat and aircraft parameters, firing patterns are stored in data memory. Data storage and retrieval are controlled by a bi-directional data bus transceiver data memory. CPU microprocessor accesses the random access memory using the address bus driver. RAM VCC provides memory power during momentary interruptions by the reset circuit. The state of the read/ write signal determines which operation (data storage or retrieval) will be done.

15-32. During normal operation and bit, the data bus transceiver discrete output applies enables to the TEWS Indicator Lights Panel. All four enables function similarly; therefore, only the MINIMUM ENABLE will be explained. On F-15C, the MINIMUM ENABLE is applied to K4 in the Avionics Miscellaneous Relay Panel No. 9. If 28VDC is available from the CMD PRGMR circuit breaker, MINIMUM relay K4 energizes and applies a ground to the deenergized contacts of advisory light test relay 52K-J219. On F-15D, the MINIMUM ENABLE is applied to MINIMUM relay 55K-Y004 in the Avionics Relay Panel No. 9. If 28VDC is available from the CMD PRGMR circuit breaker, 55K-Y004 energizes and applies a ground to the deenergized contacts of advisory light test relay 52K-J219. The ground applied to the MINIMUM light on the TEWS indicator lights panel, makes the light go on.

15-33. Firing pattern commands are sent to the DSA-R Aft, DSA-R FWD, DSA-L Aft and DSA-L FWD data input circuits. The internals of each DSA are similar; therefore, only DSA-R Aft will be discussed. The commands select the squibs to be fired, enable the fire bus to ignite the selected squib, test the firing circuits, or conduct a payload inventory. The command words are loaded into the data input when DSA INHIBIT or PWR RESET are not present. The sync decoder does a comparison test and determines if sync pulses are correct. If correct, outputs are sent to the data output and parity circuits. The command word is tested to see if the correct identification pulses for DSA-R Aft exist. If identification pulses do exist, a data output enable is produced. If identification pulses do not exist, an inhibit is applied to the parity circuit. The parity circuit outputs an even (error) signal if correct parity is not received. An odd output along with a data output enable will produce a strobe out of the AND gate to the address decoders and command timer. If PWR RESET does not exist, the strobe will enable the command timer to produce a single-short output of sufficient length to be applied to the command decoders. Lack of PWR RESET when CMD 2 output exists from the data input, enables a command timer output. The CMD 1, CMD 2 and command timer output are used by the command decoder to enable the fire bus. Whether the POLLING ENABLE, FIRE HI or FIRE LO output is produced is determined by the state of the CMD 1 and CMD 2 inputs. If the fire ENABLE is produced, a WOW ENABLE 2 is applied to the WOW ENABLE AND gate. The WOW ENABLE AND gate outputs an enable to the WOW ENABLE when WOW ENABLE 1 is available from FIRE MUX 2. If PWR RESET does not exist, the fire pwr ENABLE AND gate applies 28VDC to the fire pwr ENABLE when the L MLG WOW Relay no. 1 is energized (Weight-Off-Wheels). The 28VDC fire voltage will exist when the DSA Safety Switch -R safety pin is removed. At this time, the fire bus can be used for polling, fire lo, fire hi, or bit.

15-34. The polling command turns on the low current polling switch to provide a current path through the selected squib to 28VDC LOGIC PWR. The current is fused by F1 and insufficient to fire a squib. The voltage

across the squib is detected by the continuity circuit and an output is produced if the squib contact resistance is within tolerance. The FIRE LOW output turns on the fire switch to provide a current path through the selected squib to 28VDC fire. The fire bus voltage is limited to approximately 4.7VDC so that only the low voltage section of the selected dual chaff cartridge squib is fired. The fire hi output turns on the fire switch to provide a current path through the selected squib to the fire bus. The voltage is not limited so that either the standard squib fires or the zener diode in the selected dual chaff cartridge fires. Selection of which squib will be fired, tested, or polled (inventoried) is controlled by FIRE MUX 1 or 2.

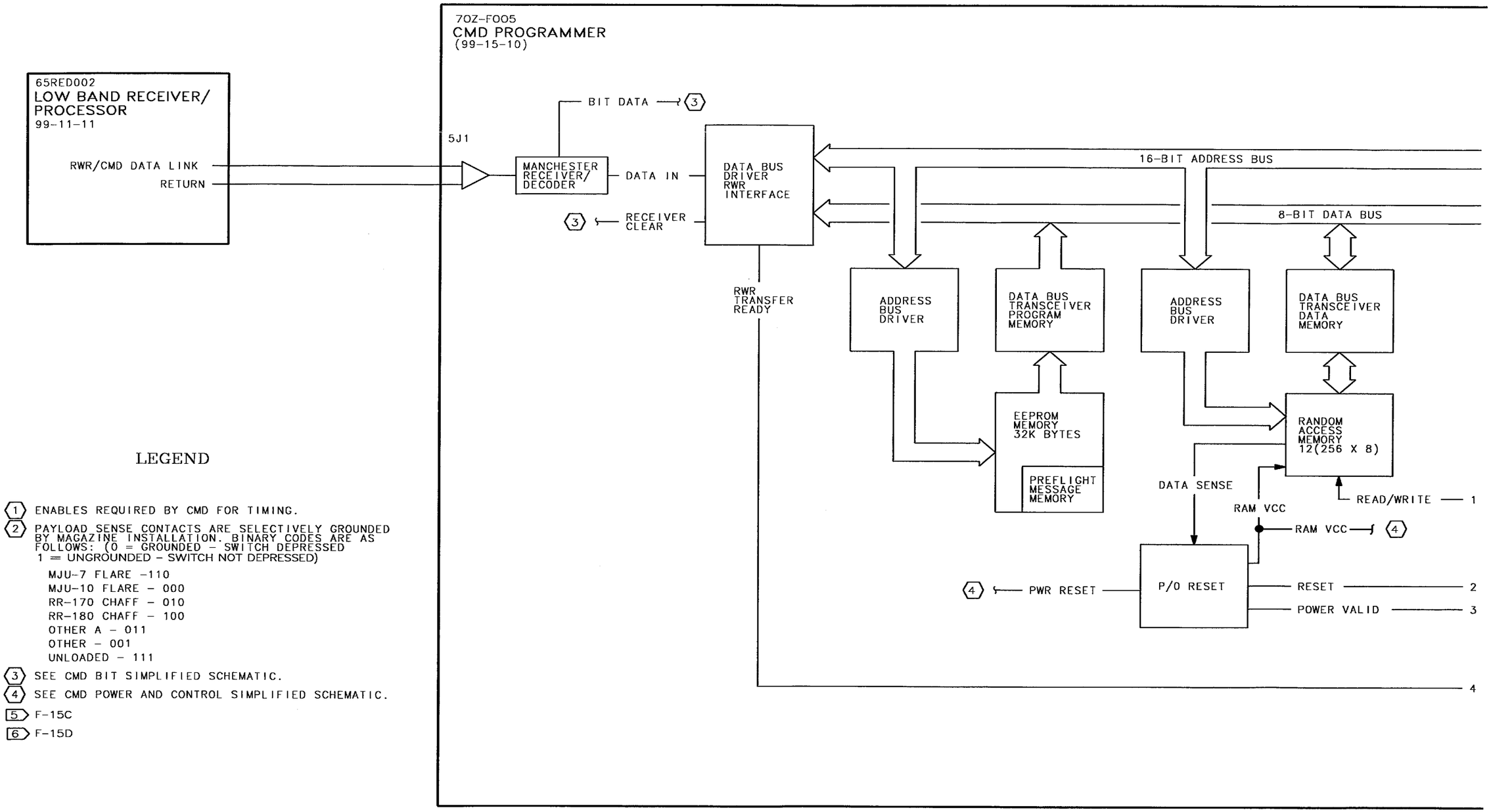
15-35. FIRE MUX 1 and 2 are controlled by the inputs to the address decoders. The address 1 and 2 inputs determine whether FIRE MUX 1 or 2 will be used to fire squibs. The resultant strobe signal is applied to the selected fire mux. Address 3, 4, 5, and 6 enable bits which select firing pins 1 thru 30. The addresses from the CPU within the programmer determine which squibs will be fired, tested for stray voltage, or counted by the continuity circuit. In addition, the address 3, 4, 5, and 6 signals produce payload out from FIRE MUX 2 and bit fire from FIRE MUX 1. Payload out identifies that an inventory is to be taken while bit fire signals the start of a mux ok test.

15-36. The DSA-R Aft has three breech plate sensing switches. The magazines containing MJU-7 and MJU-10 flare, RR-170 and RR-180 chaff, or other dispensables selectively ground the sensing switches. The ground/open signal combinations identify which dispensables are loaded. The information is outputted as payload sensor 1 and 2 signals.

15-37. **BIT.** See Figure 15-6. Three types of BIT are possible on the CMD; full initiated, initiated inventory and continuous. Full initiated BIT is done with the mode switch in STBY. Initiated inventory BIT is done with the mode switch in MAN ONLY, SEMI AUTO or AUTO position. At this time, circuits required to conduct an inventory of dispensables are used. The inventory is displayed on the TEWS display, same as full initiated BIT, less the OFP, PFM and Patch No. The remaining BIT function, continuous BIT, is done without actuation of the INITIATE switch on the BIT Control Panel. Continuous BIT is done with the mode switch in any position other than OFF. (Fault indications in continous BIT are the same as the fault indications during full initiated BIT. CMD operation is tested by display of payload, as well as, status information. If data out enable exists and even (error) does not exist, PAYLOAD SENSOR 1 and 2, DATA OUT ENABLE, CONTINUITY, and PAYLOAD OUT are applied to the payload and status output circuit. When parity is correct, the data out consisting of which dispensables are loaded (chaff, flare, or other) and the amount of each are sent to the CMD programmer. The data bus driver discrete input receives the inputs from the DSA-R Aft, DSA-L FWD, DSA-L Aft, and DSA-R FWD. The payload data is sent to the CPU microprocessor thru the 8-BIT DATA BUS when initiated by the 16-BIT ADDRESS BUS. The CPU microprocessor loads and maintains an update of payload data in the RAM using the 8-BIT DATA BUS when requested.

15-38. Full initiated BIT is activated by positioning the BCP system select switch to CMD and pressing the INITIATE switch. Upon activating the BCP INITIATE switch, a discrete signal (BIT initiate) is applied to the data bus driver discrete input in the CMD programmer. The BIT initiate is sent to the CPU microprocessor. A BIT acknowledge signal from the data bus transceiver discrete output is applied to the BCP causing the CMD light to flash for a period of the manually initiated BIT program (approximately 10 seconds). The CPU microprocessor runs several routines which test the random access and EEPROM memory, reset circuits and the CPU. microprocessor. The EEPROM then injects knowns to and compares the outputs from the data bus driver discrete input and data bus transceiver discrete output circuits. The manchester encoder/ transmitter and receiver/decoder are tested when BIT ENABLE and test data are applied by the CPU microprocessor. The threat acknowledge, program identification or request for stores cannot be transmitted at this time. A malfunction produces the door 10R (Programmer) fail signal which sets the programmer BIT fail indicator (black and white) and the ASP fault indicator 7 (orange).

15-39. Full initiated BIT also applies a bit display request to the Low Band Receiver/Processor. The Low Band Receiver/Processor sends a request for stores word. Data messages to be transmitted are loaded into RAM. When the message control receives the RWR data detect and receiver clear signals; a write output is applied to the RAM. Now, data bits are read from RAM and transmitted to the low band receiver/ processor, as long as transmit is applied from message control. The RWR displays the following information



LEGEND

(1) ENABLES REQUIRED BY CMD FOR TIMING.

(2) PAYLOAD SENSE CONTACTS ARE SELECTIVELY GROUNDED BY MAGAZINE INSTALLATION. BINARY CODES ARE AS FOLLOWS: (0 = GROUNDED - SWITCH DEPRESSED 1 = UNGROUNDED - SWITCH NOT DEPRESSED)

- MJU-7 FLARE -110
- MJU-10 FLARE - 000
- RR-170 CHAFF - 010
- RR-180 CHAFF - 100
- OTHER A - 011
- OTHER - 001
- UNLOADED - 111

(3) SEE CMD BIT SIMPLIFIED SCHEMATIC.

(4) SEE CMD POWER AND CONTROL SIMPLIFIED SCHEMATIC.

[5] F-15C

[6] F-15D

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Figure 15-5. CMD Logic and Firing Simplified Schematic (Sheet 1 of 5)

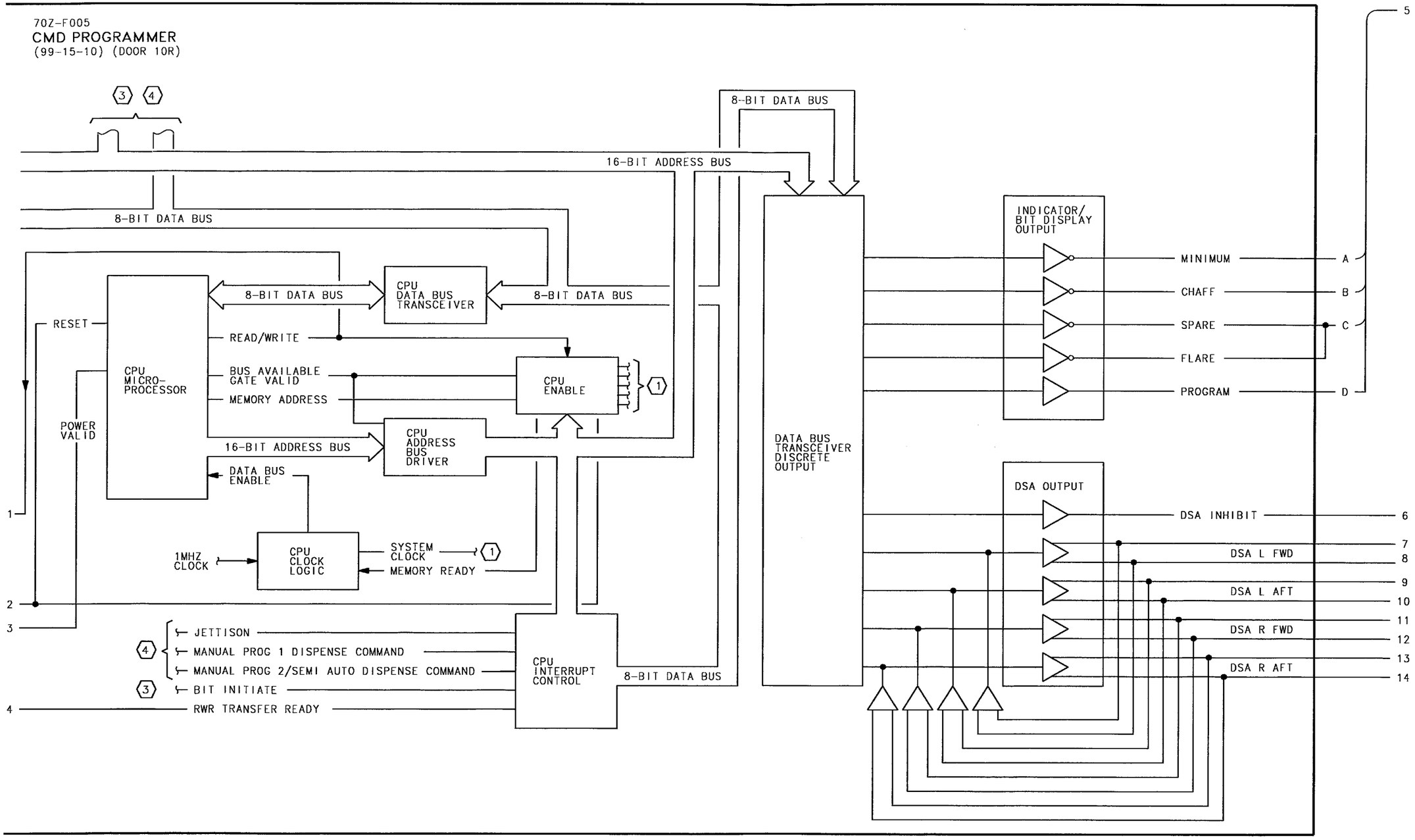

Figure 15-5. CMD Logic and Firing Simplified Schematic (Sheet 2)

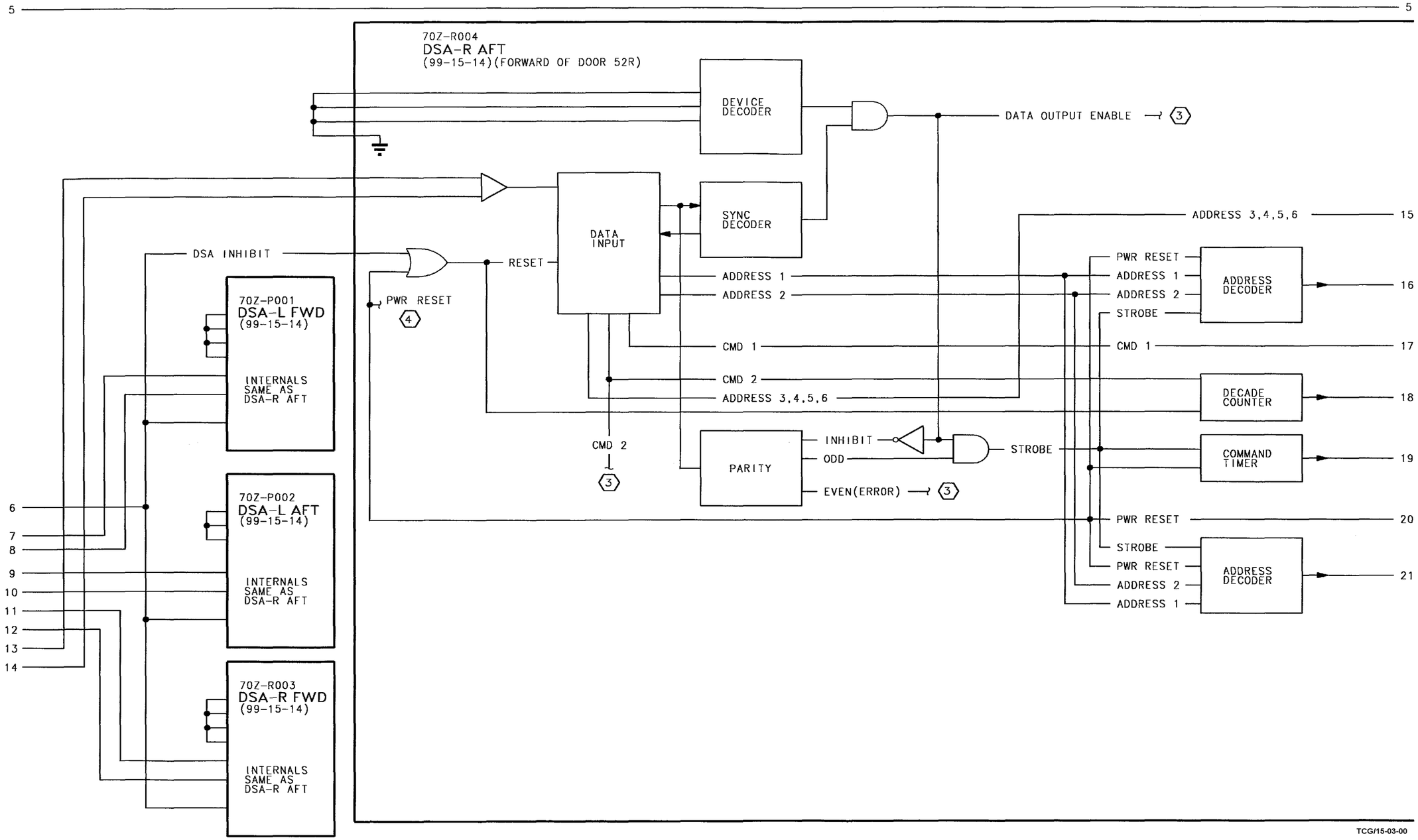

Figure 15-5. CMD Logic and Firing Simplified Schematic (Sheet 3)

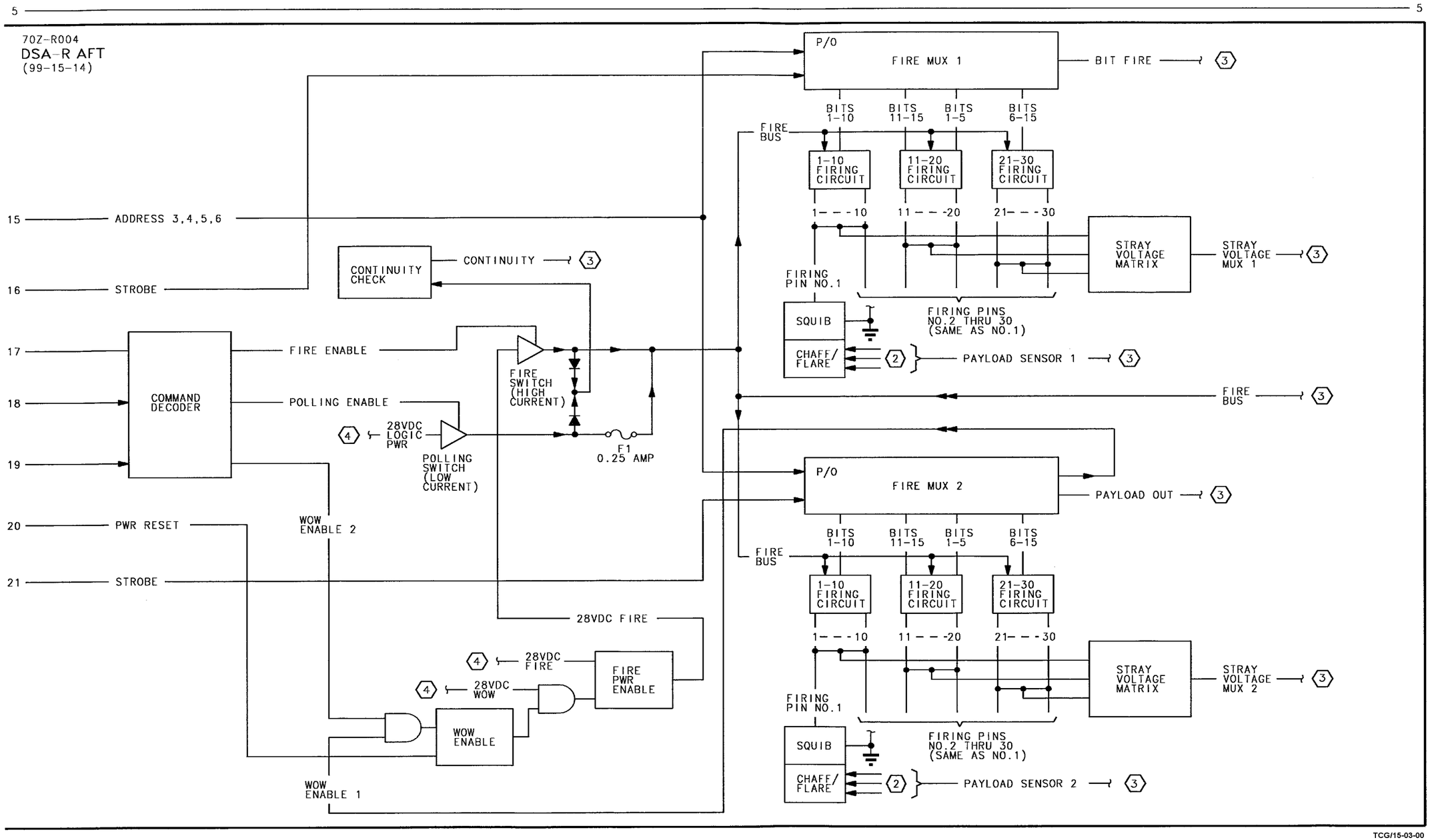

Figure 15-5. CMD Logic and Firing Simplified Schematic (Sheet 4)

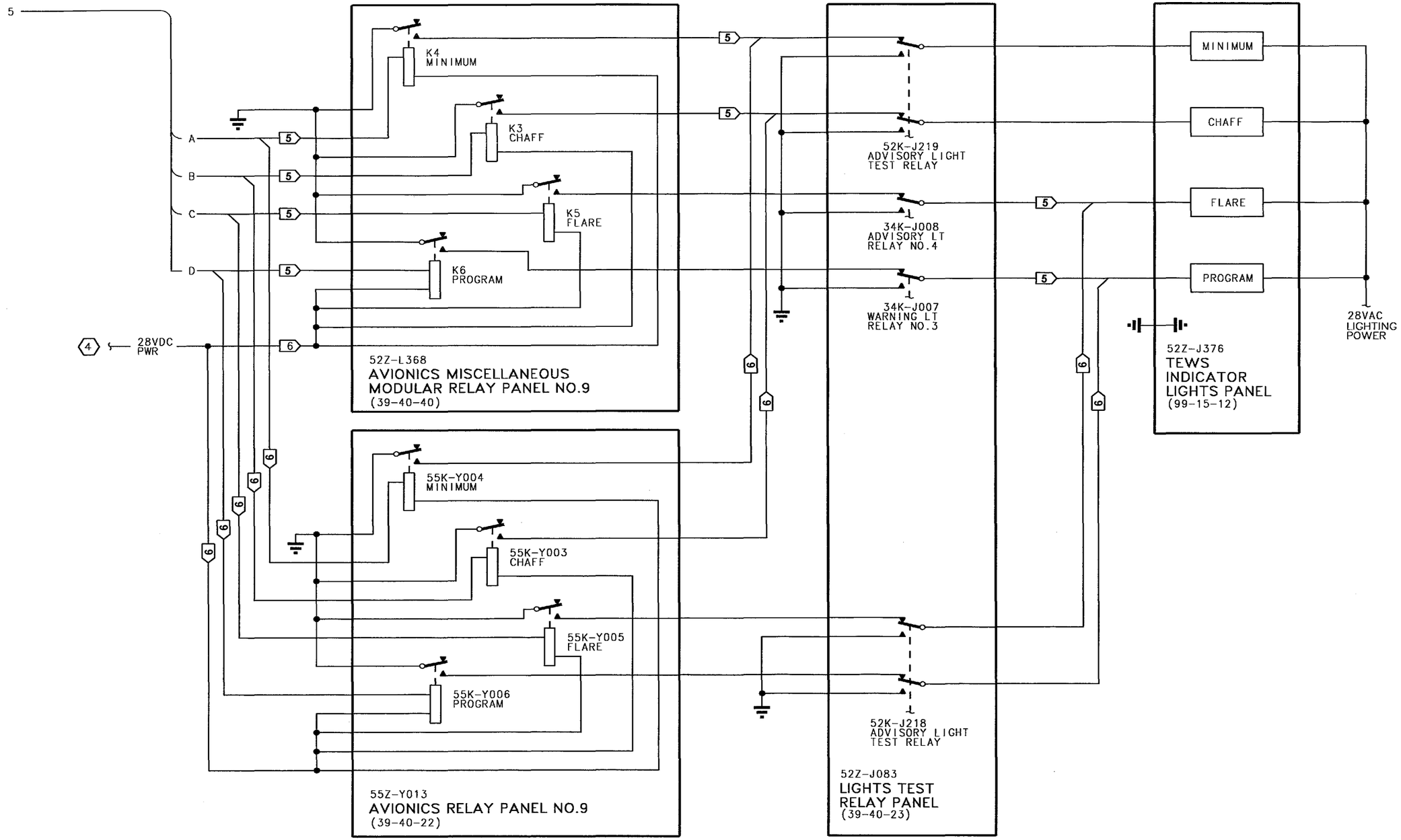

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Figure 15-5. CMD Logic and Firing Simplified Schematic (Sheet 5)

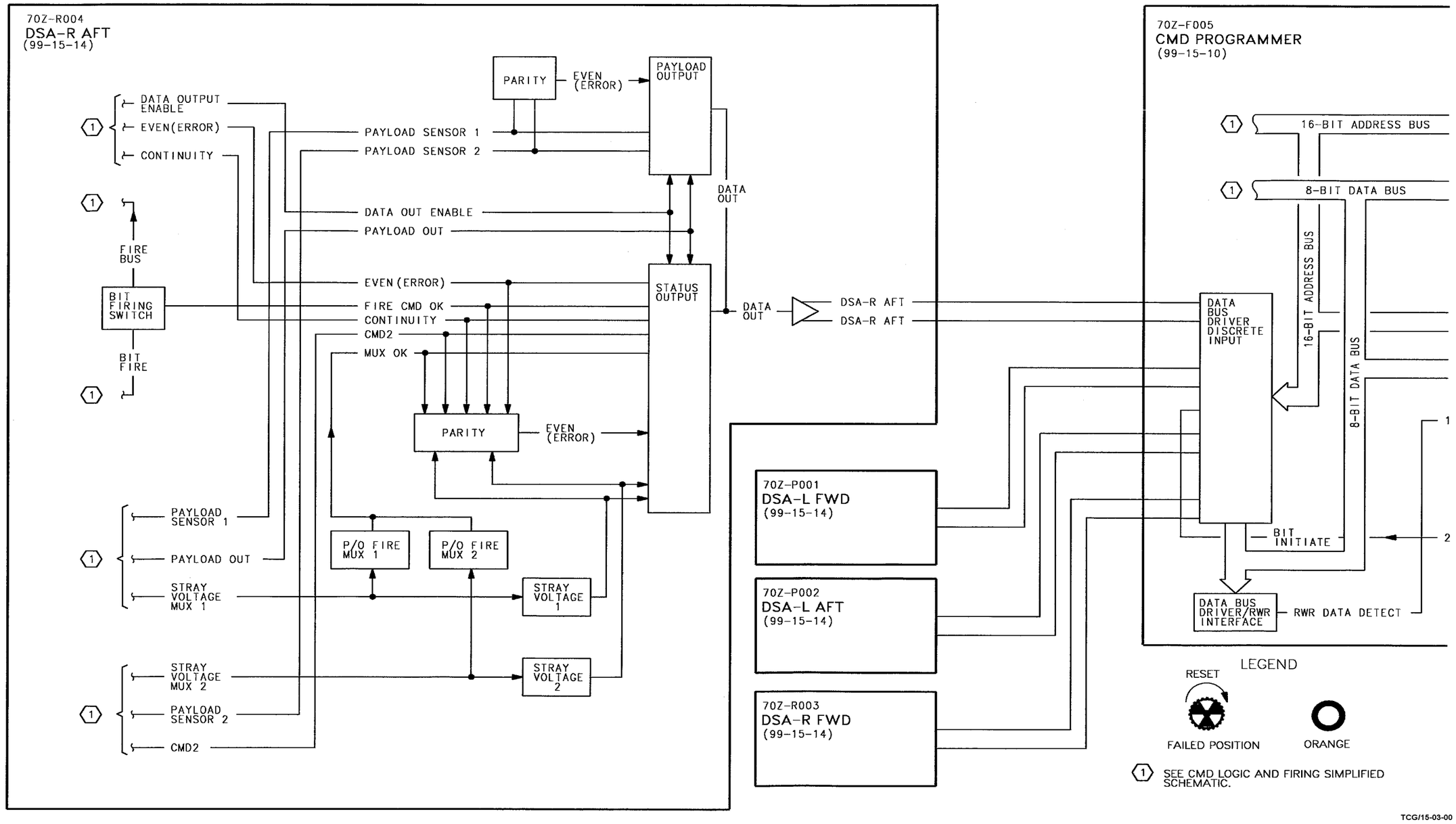


Figure 15-6. CMD BIT Simplified Schematic (Sheet 1 of 2)

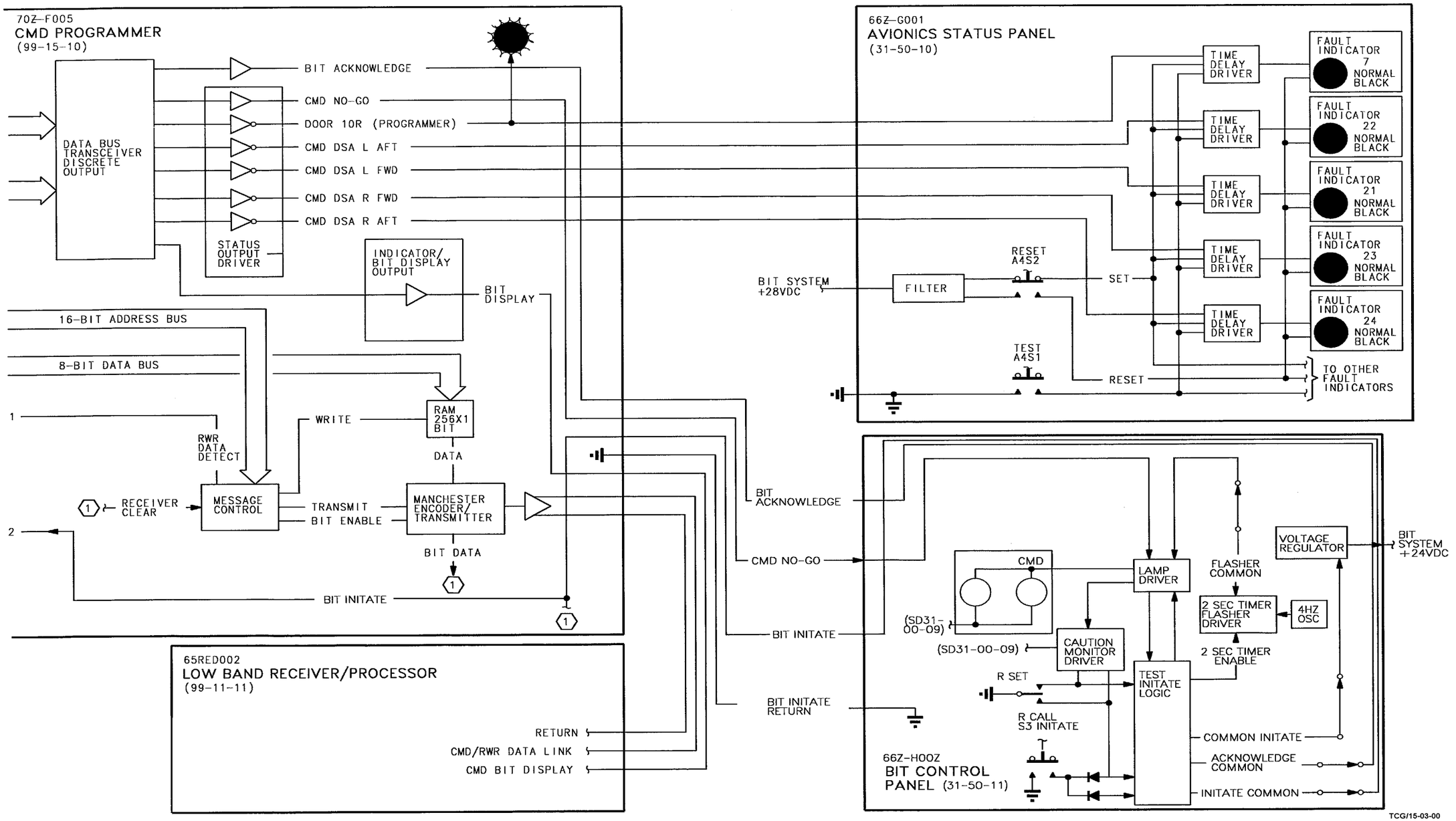


Figure 15-6. CMD Bit Simplified Schematic (Sheet 2)

on the TEWS Display Unit; OFP, PFM, Patch No., RR-170 and RR-180 Chaff, MJU-10 and MJU-7 Flare and other dispensable inventories. When the message word is transmitted, the message control removes the write and transmit signals and the sync BIT transmission is resumed.

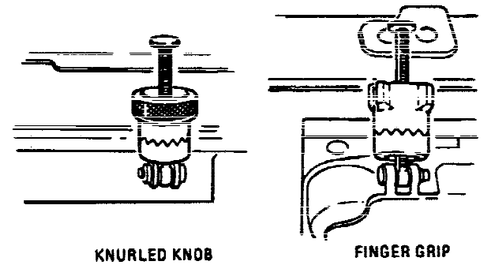
15-40. During full initiated BIT (or initial set turn on) with weight on wheels, STARY VOLTAGE MUX 1 and 2 are applied to the status output. If parity is correct, data out enable exists and payload out or CMD 2 is not enabled, the signals will be communicated to the CMD programmer. The signals sense very low levels of stray voltage at the firing pins and are used to alert the CMD programmer. If stray voltage exists, and expendable stores magazine is not installed, the CMD programmer starts the CMD no-go and applicable CMD DSA L Aft, CMD L FWD, CMD R FWD or CMD R Aft output from the data bus transceiver discrete output. The CMD NO-GO is applied to the BCP causing CMD light to come on. The other outputs set ASP fault indicators 21, 22, 23 or 24 (orange) respectively. The communication between the CMD programmer and any DSA is continuously monitored. A communication error is detected, the data driver in the CMD programmer is tested. Upon initial failure of the data driver in the CMD programmer, BIT fail indicator will set. If the failure was momentary, the CMD light will go out. If the data driver is not the reason for the communication error, ASP fault indicators 21, 22, 23, or 24 will set and the respective DSA inventory will be deleted from memory. If the number of DSA that fail exceeds the preprogrammed number, the CMD light will come on. During continuous and/or initiated BIT, if weight on wheels (WOW) inputs to the programmer and DSA do not match, then the programmer or appropriate DSA will be latched.

15-41. During full initiated BIT, DSA commands from the CMD programmer enable the BIT fire command output from FIRE MUX 1. The BIT firing switch simulates the squib load and if correct voltage exists, a FIRE CMD OK is applied to the status output and the fire bus. During this time, the fire bus is turned on and the continuity circuit is enabled. The polling command is used and each of the 60 firing pin circuits are selected, one at a time, and low level current is allowed to flow in the circuit. The outputs across the STRAY VOLTAGE MUX 1 and 2 lines are detected by the FIRE MUX 1 and 2 circuits. MUX OK indicates satisfactory selection of the firing circuits. If parity is correct, data out enable exists, even (error) and payload out are disabled; status data outputs are enabled. FIRE CMD OK, MUX OK, STRAY VOLTAGE 1 and 2 are sent to the CMD Programmer. If a malfunction exists, with weight on wheels, the CMD Programmer initiates the CMD NO-GO output. The applicable ASP fault indicators 21, 22, 23, or 24 are set orange. If a malfunction exists with weight off wheels, the CMD Programmer will produce the CMD NO-GO, only if the programmed number of DSA have all failed. Applicable ASP fault indicators 21, 22, 23, or 24 will be set orange.

15-42. **SPECIAL MAINTENANCE REQUIREMENTS.**

15-43. **FASTENERS.** Refer to applicable paragraph below.

15-44. **LRU Spring Lock Fastener Loosening and Tightening.**



CAUTION

To prevent damage to fasteners, do not use hand tools to loosen or tighten knobs.

NOTE

Two types of LRU spring lock fasteners are used. One fastener has a knurled knob and the other a knob with four finger grips.

15-45. Loosening.

1. Pull knob out to release serrated collar and turn CCW until knob no longer engages collar when released.
2. Turn knob CCW until collar can be pulled up enough to rotate swivel bolt down to clear mounting foot on LRU.

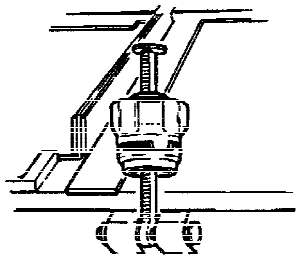
15-46. Tightening.

1. Rotate swivel bolt up until serrated collar

2. Turn knob CW until knob is tight.

3. Gently rock LRU and turn knob until tight.

15-47. **LRU Ratchet Fastener Loosening and Tightening.**



CAUTION

To prevent damage to fasteners, do not use hand tools to tighten or loosen knobs.

15-48. Loosening.

1. Turn knob CCW until swivel bolt can be rotated to clear mounting foot on LRU.

15-49. Tightening.

1. Rotate swivel bolt up to engage LRU mounting foot.
2. Turn knob CW to tighten knob.
3. Gently rock LRU and turn knob until tight.

15-50. **CONSUMABLE MATERIALS LIST.**

15-51. **SUPPLIES (CONSUMABLES).** A list of supplies required to support the organizational maintenance of the CMD system is provided in Table 15-3.

Table 15-3. Supplies (Consumables

System/ Nomenclature	Material	Part Number (Mfg. Code)
Lockwire	Monel	MS20995NC32 (96906)

15-52. **SUPPORT EQUIPMENT LIST.**

15-53. **TEST EQUIPMENT.** Test equipment required for maintenance of the CMD system is listed in Table 15-4.

Table 15-4. Test Equipment List

System/Equipment Number	Nomenclature	Use and Application
AN/ASM-700	Program Loader Verifier Test Set	Refer to 99-15-03, 99-15-05
AN/PSM-37	Mulitmeter	Trouble analysis
AN/PSM-6( ) (Alternate)		
4920-01-149-248	Dispenser Switch Assembly Protector	Safe transport of Dispenser Switch Assemblies

GLOSSARY

Nonstandard abbreviations and symbols are described below. All abbreviations and symbols used in the maintenance manual set are described in TO SR1F-15C-2-00GV-00-1.

ABBREVIATIONS

AI	Airborne Intercept
ALC	Automatic Leveling Circuit
ASP	Avionics Status Panel
ATAK	Attack/offensive
ATU	Agile Tuning Unit
BCP	BIT Control Panel
BIT	Built in Test
CC	Central Computer
CMD	Countermeasures Dispenser Set
CPU	Central Processing Unit
DF	Direction Finding
DFNS	Defensive
DSA	Dispenser Switch Assembly
DTM	Data Transfer Module
ECS	Environmental Control System
EEPROM	Electronic Erasable Programmable Read Only Memory
IA	Immediate Action
ICMS	Internal Countermeasures Set
IRS	Improved Radar Simulator
LRU	Line Replaceable Unit
MAU	Modulation Analysis Unit
MPCD	Multipurpose Color Display
MPFM	Missionized Pre-flight Message
MSS	Mission Support System
MU	Memory Unit
OFP	Operational Flight Program
PFM	Preflight Message
PGM	Program
PLV	Program Loader Verifier
PRF	Pulse repetition Frequency
PROM	Programmable Read Only Memory
RFA	RF Amplifier
ROM	Read Only Memory
RTU	Repeater Unit
RWR	Radar Warning Receiver
SAW	Surface Acoustic Wave
SIM	SORD Insurance Module
SORD	System Operational Requirements Document
SPU	Spurious
TEWS	Tactical Electronic Warfare System
TCU	Time Correlation Unit
TU	Tuning Unit
TWS	Track While Scan
YIG	Yttrium-Iron-Garnet (Oscillator, Multiplier, etc)
*	Indicates a low level output is the enabling signal